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ZT 8905/8906

Single Board Computer with Pentium® Processor

H A R D W A R E M A N U A L

For ZT 8905 Revision A.3

For ZT 8906 Revision A.3

ZIATECH CORPORATION

ZT M8905
September 9, 1997
102575

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ZIATECH CORPORATION

1050 Southwood Drive • San Luis Obispo, CA 93401 USA • Tel (805) 541-0488 • FAX (805) 541-5088

Central Regional Office
7700 Chevy Chase Drive, Suite 110-A
Austin, TX 78752 USA
Tel (512) 458-3177
FAX (512) 458-3178

Eastern Regional Office
319 North Pottstown Pike, Suite 107
Exton, Pennsylvania 19341 USA
Tel (610) 524-9070
FAX (610) 524-9072

European Office
P.O. Box 110
AC SON
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WHAT'S IN THIS MANUAL?

This manual describes the operation and use of the ZT 8905/8906 Single Board Computer with Pentium Processor. The term ZT 8905 is used throughout this manual to reference both the ZT 8905 and the ZT 8906, except where otherwise noted. Specific differences between the two are explicitly stated. The following summarizes the focus of each major section in this manual.

Chapter 1, "Introduction," introduces the key features of the ZT 8905. It includes a product definition, a list of product features, a functional block diagram, and a brief description of each block. This chapter is most useful to those who wish to compare the features of the ZT 8905 against the needs of a specific application.

Chapter 2, "Getting Started," summarizes the information needed to install and configure your ZT 8905.

Chapter 3, "STD 32 Bus Interface," presents a detailed description of the ZT 8905 interface to the STD 32 bus architecture. The topics discussed include compatibility, interrupt structure, and multiple master operation.

Chapter 4, "Interrupt Controller," describes the two Intel-compatible 8259 cascaded interrupt controllers. This chapter summarizes and illustrates the interrupt sources and the interrupt controllers' programmable registers.

Chapter 5, "Counter/Timers," discusses the three programmable counter/timers. It includes a diagram of the counter/timer architecture, a summary of operating modes, and descriptions of the programmable registers.

Chapter 6, "DMA Controller," provides an overview of ZT 8905 DMA architecture and DMA controller operation. Descriptions of DMA controller programmable registers are also included.

Chapter 7, "Real-Time Clock," lists the major features of the real-time clock and provides register descriptions.

Chapter 8, "Serial Controller," discusses operation of the two serial ports and provides register descriptions.

Chapter 9, "IEEE 1284 Parallel Port Interface," contains descriptions of the programmable registers for the IEEE-1284 compatible printer interface.

Chapter 10, "Optional IDE Interface," covers the mounting and enabling of an optional local Intelligent Drive Electronics (IDE) interface. It also discusses the types of configurations in which the addition of a local hard disk can be an advantage.

Chapter 11, "System Registers," provides register descriptions and a brief overview of the System registers used to control and monitor a variety of functions on the ZT 8905.

Chapter 12, "Watchdog Timer," explains operation of the watchdog timer and includes code for arming and strobing the timer.

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Chapter 13, "PCI Mezzanine Local Bus," introduces the features of the Peripheral Component Interconnect (PCI) local bus interface that provides a high speed path between the CPU and peripherals.

Chapter 14, "Programmable LED," provides code for turning the LED on and off.

Appendix A, "Board Configuration," describes the software configuration registers, jumpers, and cuttable traces on the ZT 8905. This appendix details factory default settings as well as information to tailor your board to a specific application.

Appendix B, "Specifications," contains the electrical, environmental, and mechanical specifications for the ZT 8905. It also provides illustrations of cables and connector pinouts, and tables showing connector pin assignments.

Appendix C, "Customer Support," offers a product revision history, technical assistance and warranty information, and the necessary information should you need to return your ZT 8905 for repair.

Appendix D, "PCI Configuration Space Map," presents the generic layout of the PCI Configuration Header for all PCI compliant devices. It also contains a table showing the PCI bus mapping of the ZT 8905's on-board devices.

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CHAPTER 1. INTRODUCTION

This chapter provides a brief introduction to the ZT 8905. It includes a product definition, a list of product features, a functional block diagram, and a description of each block. Unpacking information and installation instructions are found in Chapter 2, "Getting Started."

PRODUCT DEFINITION

The term ZT 8905 is used throughout this manual to reference both the ZT 8905 and the ZT 8906, except where otherwise noted. Specific differences between the two are explicitly stated. Refer to Appendix B for specifications.

ZT 8905

The ZT 8905 is a highly integrated, single board computer that is factory configured to operate with the Pentium® (P54C) family of microprocessors. The board meets the needs of a wide range of industrial control and processing applications by operating stand alone, as a single master in an STD 32® architecture, or as a permanent or temporary master in an STD 32 STAR SYSTEM™ architecture. High speed peripheral operation is provided by an on-board PCI expansion interface.

ZT 8906

The ZT 8906 is physically a ZT 8905 with a three-slot CompactPCI™ enclosure attached to it. This enclosure allows high-speed PCI peripherals to be used as a processing core, yet allows access to the STD 32 Bus architecture for I/O available on that bus structure.

All other features of the ZT 8906 are identical to the ZT 8905 unless otherwise noted in this manual.

The following topics discuss stand-alone, STD 32 single master, and STD 32 multiple master (STAR SYSTEM) operation.

Stand Alone

The ZT 8905 does not require an STD bus backplane to operate. The ZT 8905 is able to operate stand-alone in many applications because of the large selection of the most commonly needed peripheral devices. On-board peripheral devices include:

- 2 or 4 Mbyte Flash file system for disk support
- PCI local bus expansion port (CompactPCI compliant)
- Optional IDE hard disk interface
- Keyboard controller
- Serial I/O
- Speaker interface
- Interrupt controllers
- Counter/timers
- Watchdog timer
- Real-time clock

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STD 32 Single Master

The ZT 8905 supports additional memory and I/O through the STD 32 bus. Both Standard Architecture (8- and 16-bit) and Extended Architecture (8-, 16-, and 32-bit) transfer types are dynamically supported through the STD 32 interface. Jumperless configuration of interrupt, DMA, and STD 32 bus memory and I/O space is configured through the BIOS SETUP utility. See the section "ZT 8905 SETUP" in Chapter 2 for more information.

STD 32 Multiple Master (STAR SYSTEM)

The ZT 8905 is configurable to operate in a multiple master architecture as a Permanent Master or a Temporary Master. With this architecture, up to seven ZT 8905 boards share STD bus memory and I/O resources. The Permanent Master provides the system clock and reset function and also provides the pull-up signals for the open-collector signals on the STD 32 bus. The Permanent Master is also responsible for initializing shared memory and other system I/O on behalf of any Temporary Masters. The STAR BIOS manages all of the system initialization.

FEATURES OF THE ZT 8905

- STD 32 bus compatible
- PCI compatible local bus (CompactPCI compliant)
- Single and multiple master operation
- Pentium processor CPUs to 200 MHz
- Numeric coprocessor support (Pentium)
- 16 Kbytes of CPU cache (expandable with L2 cache)
- Optional IDE hard disk interface (local to ZT 8905)
- 8, 16, 32, or 48 Mbytes of DRAM memory
- 2 Mbytes of Flash memory (expandable to 4 Mbytes)
- Optional 32-bit PCI local bus peripheral support (through CompactPCI)
  - --Super VGA (640x480x16M through 1280x1024x64K)
  - --Contact Ziatech for additional peripherals
- Standard AT® peripherals include:
  - --Two enhanced interrupt controllers (8259)
  - --Three counter/timers (one 8254)
  - --Real-time clock/CMOS RAM (146818)
  - --Two enhanced DMA controllers (8237)
  - --8042 compatible keyboard controller
- Centronics printer port (ECP/EPP compatible)
- Two 16C550 RS-232 serial ports
- Single stage watchdog timer
- Speaker interface

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- On-board high efficiency 3.3 V DC-DC converter
- Push-button reset
- Software programmable LED
- DC power monitors (3.3 V and 5 V)
- Compatible with the following software: MS-DOS®, OS/2®, UNIX®, QNX®, VRTX32®, Windows™ 3.1 and 3.11, Windows 95, and Windows NT
- DOS and STAR BIOS options
- STD 32 bus standard 4.5" x 6.5" board format
- +5 V-only operation (fan/heatsink requires +12 V)
- Burned in at 55° Celsius and tested to guarantee reliability
- Five-year warranty

DEVELOPMENT CONSIDERATIONS

Ziatech offers two software development systems for ZT 8905 applications: DOS and the STD 32 STAR SYSTEM.

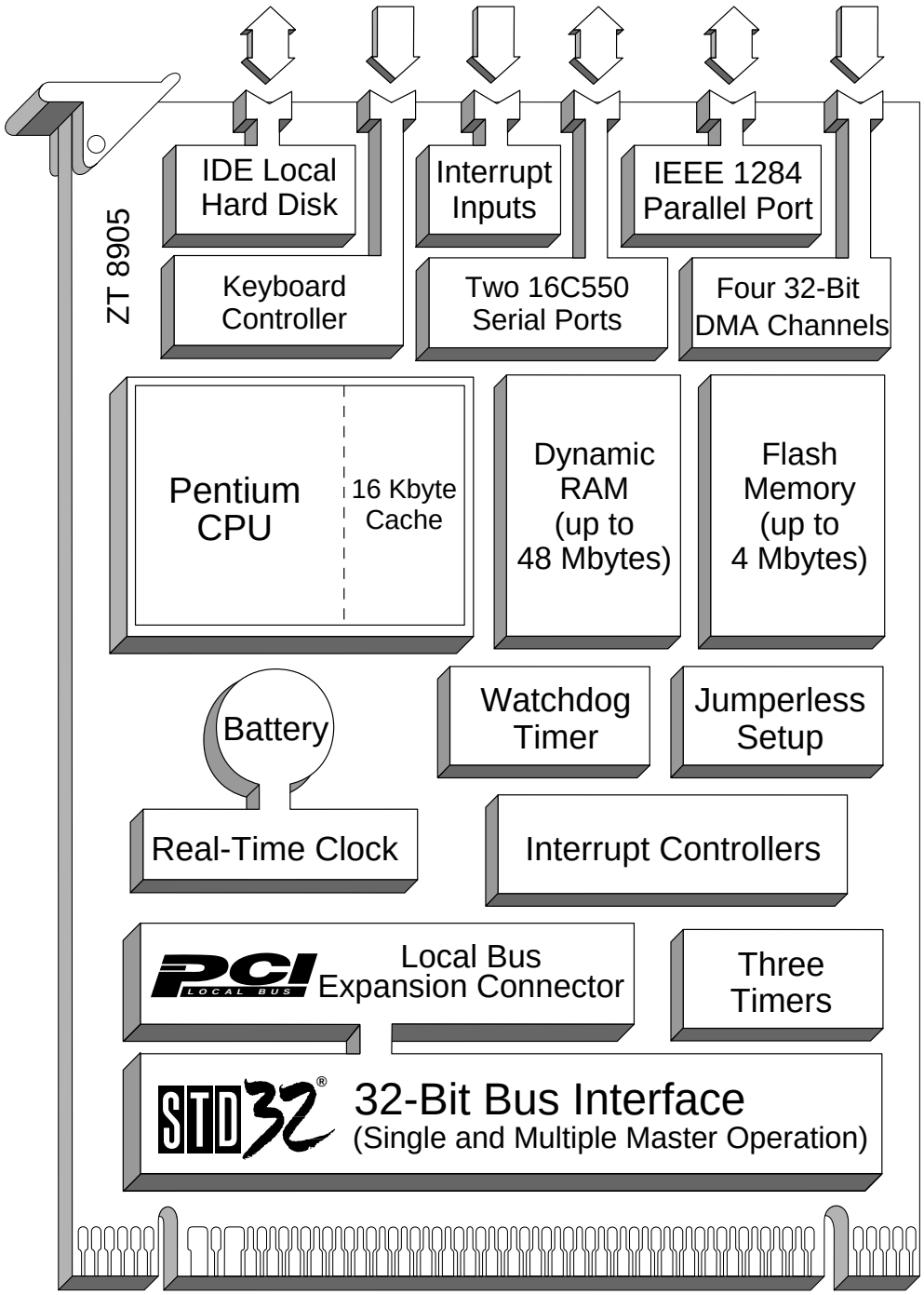
Ziatech DOS is Microsoft's MS-DOS residing on the ZT 8905. The DOS system provides a development platform similar to a PC, enabling applications to be developed quickly. DOS includes support for many of the ZT 8905 peripherals and is supported by a large number of development tools such as program editors, compilers, assemblers, and debuggers. Refer to the Ziatech system manual for configuration and operating instructions.

The STD 32 STAR SYSTEM is the DOS platform operating on more than one master in a single STD bus system. Each master includes local memory, local I/O, and the DOS operating system. Each master is capable of sharing STD bus memory and I/O, such as fixed disks, floppy disks, and video. Refer to the STAR SYSTEM operating manual for configuration and operating instructions.

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FUNCTIONAL BLOCKS

The "Functional Block Diagram" below illustrates the board's major functional blocks. The topics that follow provide overviews of the functional blocks.



Functional Block Diagram

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STD 32 Bus Interface

The ZT 8905 operates in the STD 32 system. In an STD 32 system, data transfers are dynamically sized for either 8- or 16-bit Standard Architecture or 8-, 16-, or 32-bit Extended Architecture transfers. All STD-80 compatible memory and I/O boards are supported using 8-bit Standard Architecture transfers. STD 32 compatible memory and I/O boards are dynamically sensed to determine the width of the data transfer.

The STD 32 system provides the platform needed for multiple master operation. In a multiple master system, up to seven ZT 8905 boards share STD bus resources with a fixed or rotating priority granted by an external bus arbiter, such as the ZT 89CT39.

See Chapter 3, "STD 32 Bus Interface" for a detailed description of the ZT 8905 interface to the STD 32 bus architecture. The topics discussed include compatibility, interrupt structure, and multiple master operation.

Pentium Processors

The ZT 8905 supports the second generation Pentium processor family, commonly referred to as the P54C. The P54C is a 3.3 V processor and operates at higher frequencies and lower power than did the first generation Pentium (P5). The ZT 8905 operates the external microprocessor bus at either 50, 60, or 66 MHz. The P54C operates internally at 1.5x, 2x, 2.5x, or 3x the microprocessor bus, supporting potential Pentium internal operation at up to 200 MHz.

The "Pentium Processor Comparison" table below indicates the possible operating frequencies of the ZT 8905. The PCI bus always operates at 1/2 the external microprocessor bus speed. Not all processor speeds are offered by Ziatech, nor will Intel necessarily offer all speeds below. Contact Ziatech for latest product offerings.

The Pentium processor includes 16 Kbytes of cache (referred to as L1 cache). This L1 cache supports both write-through and write-back cache. A secondary cache (L2 cache) option is planned to further enhance memory performance. Contact Ziatech for details on availability of the L2 cache option.

Pentium Processor Comparison

Processor Speed (MHz)	Internal Clock Multiplier	External Processor Speed	PCI Operating Frequency
90	1.5X	60.0	30.0
100	1.5X	66.6	33.3
120	2.0X	60.0	30.0
133	2.0X	66.6	33.3
150	2.5X	60.0	30.0
166	2.5X	66.6	33.3
180	3.0	60.0	30.0
200	3.0	66.6	33.3

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Memory and I/O Addressing

The ZT 8905 includes two 72-pin sockets that support up to 48 Mbytes of DRAM. The ZT 8905 also supports Flash memory soldered directly on the board. Memory operations that are not decoded for on-board DRAM are forwarded to the STD 32 bus. EA memory interfaces (for example, ZT 8920) may be mapped anywhere above local memory space in the 32-bit EA address space. SA peripherals are limited to the lower 16 Mbyte address space because the SA memory address range is only 24 bits in depth. If 16 Mbytes or more of local DRAM are loaded on the ZT 8905, then SA peripherals can only be located in the lower 1 Mbyte address space. STD 32 memory addressing is configured through the BIOS SETUP utility. For more information, see the topics "Memory Configuration" and "ZT 8905 SETUP" in Chapter 2.

The ZT 8905 also includes many I/O peripherals required for industrial control applications. 8- and 16-bit SA I/O peripherals are supported. 8-, 16-, and 32-bit EA I/O is also supported. For both SA and EA I/O, addressing is limited to 64 Kbytes (16 bits). The IOEXP signal is dynamically driven low in the FC00h-FFFFh address range to allow older STD I/O boards that decode less than 16 bits of address from being redundantly mapped. STD 32 peripherals can be located in the 100h-1FFh, 200-2FFh, 300h-3FFh, and 8000h-FFFFh (E000h-FFFFh for pre-Revision A.2 boards) address spaces. These regions are configurable through the BIOS SETUP mechanism. For more information, see "I/O Configuration" in Chapter 2.

PCI Local Bus

The ZT 8905 supports high speed peripheral interfacing via a PCI mezzanine interface. The mezanine is implemented through a high density 2 mm connector provided by the ZT 8905. 32-bit PCI is supported by the ZT 8905 PCI connector. The mezzanine board size is 51 mm x 135 mm. When the mezzanine board is attached to the ZT 8905, the overall height of the mezzanine is 12.5 mm, allowing the mezzanine board/ZT 8905 combination to occupy just one total STD 32 slot space. Note that the fan/heatsink option for the Pentium will require two total slots.

The ZT 8905 additionally supports a pass-down connector for video signals from VGA mezzanine boards such as the zPM10 Super VGA Interface. The video signals are then routed to the multi-I/O connector interface on the ZT 8905 for display interfacing. See Chapter 13, "PCI Mezzanine Local Bus," for more details on the PCI interface.

Serial I/O

Two 16C550 PC-compatible serial ports are available. The serial ports are implemented with a 5 V charge pump technology to eliminate the need for a ±12 V supply. Both serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115.2 Kbaud.

The serial ports are configured as DTE and are available through the multi-I/O frontplane connector. The ZT 90205 cable converts the multi-I/O interface to a standard 9-pin D-shell connector. A null-modem option is available to convert the DTE configuration to DCE. Adapter board options are also available to convert the RS-232 interface to an RS-485 interface. For more information on ZT 8905's serial ports, see Chapter 8, "Serial Controller."

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Interrupts

Two enhanced 8259 style interrupt controllers provide a total of 15 interrupt inputs. Interrupt controller features include support for level-triggered and edge-triggered inputs, fixed and rotating priorities, and individual input masking. Interrupt sources include counter/timers, serial I/O, real-time clock, keyboard, printer, and multiple master communications. There are also five frontplane and five backplane interrupt sources. Enhanced capabilities include the ability to configure each interrupt level for active high going edge or active low level inputs.

All interrupt routing for STD 32 and frontplane interrupt sources is done through the BIOS SETUP utility, allowing jumperless configuration (See "ZT 8905 SETUP" in Chapter 2 for more information). The PCI enumerator can also configure up to four PCI interrupts.

See Chapter 4, "Interrupt Controller," for more information on the ZT 8905's two interrupt controllers. This chapter summarizes and illustrates the interrupt sources and the interrupt controllers' programmable registers.

Counter/Timers

Three 8254 style counter/timers are included on the ZT 8905 as defined for the AT. Operating modes supported by the counter/timers include interrupt on count, frequency divider, square wave generator, software triggered, hardware triggered, and one shot. See Chapter 5, "Counter/Timers," for more information.

DMA

Two enhanced 8237 style DMA controllers provide a total of one STD 32 and three frontplane DMA channels for data transfers between system I/O and local memory. The DMA channels support STD 32 bus DMA slaves by managing the data transfers between the slaves and local memory. Additional features of the DMA channels include auto initialization, address increment or decrement, and software DMA requests. Enhanced DMA capabilities include support for higher speed (8 Mbyte/sec) transfer types and 32-bit memory addressing.

One DMA channel is available through the STD bus BUSRQ* and BUSAK* signals. This is configurable as either an 8-bit DMA channel (DRQ2) used primarily for floppy disk operation or a 16-bit DMA channel (DRQ5). Three additional DMA channels are available through the Multi-I/O connector.

See Chapter 6, "DMA Controller" for more information.

Watchdog Timer

The watchdog timer optionally monitors system operation. Failure to strobe the watchdog timer within a set time period results in a system reset. Chapter 12, "Watchdog Timer" explains operation of the watchdog timer and includes code for arming and strobing the timer.

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Real-Time Clock

The real-time clock performs timekeeping functions and includes 256 bytes of general-purpose battery-backed CMOS RAM. Timekeeping features include an alarm function, a maskable periodic interrupt, and a 100-year calendar. The system BIOS uses a portion of this RAM for BIOS SETUP information (see "ZT 8905 SETUP" in Chapter 2 for more on the BIOS SETUP).

Chapter 7, "Real-Time Clock" lists the major features of the real-time clock and provides register descriptions.

Keyboard Controller

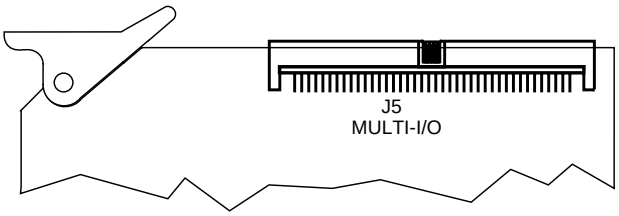
The ZT 8905 includes a PC/AT® keyboard controller that can be used instead of an off-board keyboard controller. The BIOS configures the ZT 8905 for on-board keyboard operation when an on-board PCI VGA interface is installed. Otherwise, the ZT 8905 uses the off-board keyboard controller.

IEEE® 1284 Parallel Port/Printer Interface

The ZT 8905 includes an IEEE® 1284 compatible parallel port for connection to a printer or other parallel port devices such as software keys required by many application packages. The parallel port is ECP/EPP compatible.

The printer interface is available through the multi-I/O connector (illustrated below). An optional cable (ZT 90202 for Revision 0, ZT 90205 for boards that are Revision A and higher) is available to interface the frontplane connector to a 25-pin D-shell connector for software key or printer support. The mode (Normal, Extended, EPP, ECP) for the printer interface is selectable through the BIOS SETUP utility (see "ZT 8905 SETUP" in Chapter 2 for more on the BIOS SETUP).

Chapter 9, "IEEE 1284 Parallel Port Interface," contains descriptions of the programmable registers for the IEEE-1284 compatible printer interface.



ZT8905F01-03

J5 Multi-I/O Connector

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Speaker Interface

The ZT 8905 supports an external AT-compatible speaker through the multi-I/O frontplane connector (illustrated on previous page).

Optional IDE Interface

The ZT 8905 can be ordered (Option D1) with an on-board IDE interface connector for connection to an IDE hard drive. This option is useful for single board operation (without the STD 32 backplane) or for STAR SYSTEM operation where it is desired to have a local boot device that is independent of other STAR SYSTEM CPUs. This option includes a 2.5" IDE interface mounted on a carrier board which is attached to the bottom side of the ZT 8905. When used in the STD 32 chassis, the IDE drive occupies one slot more than the standard ZT 8905. The disk carrier board also provides attachment points for single board operation, allowing the OEM an easy way of mounting the ZT 8905. See Chapter 10, "Optional IDE Interface," for more information.

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CHAPTER 2. GETTING STARTED

This chapter summarizes the information needed to make the ZT 8905 operational. You should read this chapter before attempting to use the board.

UNPACKING

Please check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Ziatech for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Do not return any product to Ziatech without a Return Material Authorization (RMA) number. Appendix C explains the procedure for obtaining an RMA number from Ziatech.

WHAT'S IN THE BOX?

The items listed below are included with a ZT 8905/8906 order. System level products, such as the DOS and STAR SYSTEM packages, include additional items not shown. If a system level product has been ordered, refer to the system manual for the packing list.

- ZT 8905/8906 Single Board Pentium Computer in anti-static bag (save the anti-static bag for storing or returning the ZT 8905/8906)
- On-Line Help disk for ZT 8905/8906
- Optional PCI peripherals
- Optional cables
- Optional paper version of user's manual

WARNING!

Like all equipment utilizing MOS devices, the ZT 8905/8906 must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the ZT 8905/8906 to handle the board.

SYSTEM REQUIREMENTS

The ZT 8905 is designed for use with or without an STD 32 bus backplane. The ZT 8905 is electrically, mechanically, and functionally compatible with the *STD 32 Bus Specification and Designer's Guide* (ZT MSTD32) for STD bus applications.

Ziatech recommends vertical mounting. The ZT 8905 is supplied with an integrated fan/heatsink to allow operation between 0° and 55° C ambient. Refer to Appendix B for additional specifications.

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MEMORY CONFIGURATION

The ZT 8905 addresses up to 4 Gbytes of memory. The address space is divided between memory local to the board, memory located on the PCI expansion interface, and memory on the STD bus. Any memory not reserved or occupied by a local memory device (DRAM/Flash) or the STD bus is available for PCI bus expansion. The memory address regions available for the STD bus are configured through the BIOS SETUP mechanism. During local memory operations, the STD bus is held static to decrease system electrical noise and power consumption.

STD bus memory is supported through either Standard Architecture (SA8 or SA16) transfers, or Extended Architecture (EA8, EA16, or EA32) transfers. The ZT 8905 supports the STD bus wait request signal, WAITRQ*, to interface to SA memory boards with longer access time requirements than those defined by the STD-80 and STD 32 specifications. The signal EXRDY is supported for EA peripherals that require additional transfer time.

The ZT 8905 is populated with several memory devices. Local DRAM is contained in a unique stackable memory architecture that supports up to 48 Mbytes of DRAM (using 16-Mbit DRAM technology). Each module is either 4 Mbytes or 8 Mbytes. Memory modules must be added in pairs due to the 64-bit memory architecture of the Pentium processor. Each layer of DRAM (up to three layers) must be configured differently to allow the stacked module to provide discrete addressing for the layer pair.

Additional DRAM may be installed on the ZT 8905 after the system has been purchased. Before contacting Ziatech to order additional DRAM, please take a moment to determine the amount of DRAM that is already loaded (how many layers and what size). The "Typical DRAM Configurations" table below lists the typical DRAM configurations that are possible with the ZT 8905. Single sided DRAM modules have DRAM on just one surface. Double sided DRAM modules have DRAM on both sides.

Local Flash memory is soldered directly to the board. There is space for one Flash device, which may be either a 2 Mbyte or a 4 Mbyte device. The 2 Mbyte device does not require +12 V operation. The 4 Mbyte device does require +12 V +/- 5% for programming operations.

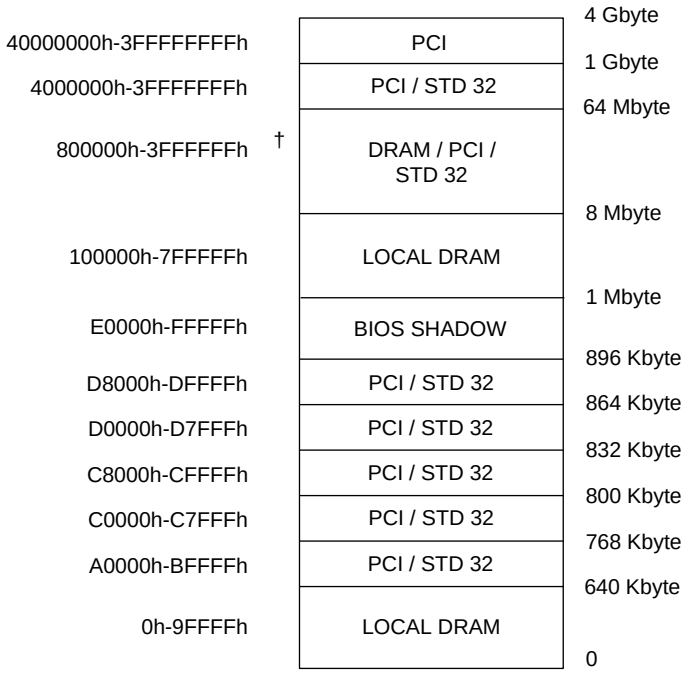
The "Memory Address Map" illustration on the following page shows default memory addressing for the ZT 8905.

Typical DRAM Configurations

Total System Memory	Number and Type of Modules
8 Mbytes	Two 4-Mbyte modules (layer 1)--single sided
16 Mbytes †	Four 4-Mbyte modules (layers 1 & 2)--single sided
16 Mbytes	Two 8-Mbyte modules (layer 1)--double sided
32 Mbytes	Four 8-Mbyte modules (layers 1 & 2)--double sided
48 Mbytes	Six 8-Mbyte modules (layers 1, 2 & 3)--double sided

† Upgraded systems only

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Memory Address Map

I/O CONFIGURATION

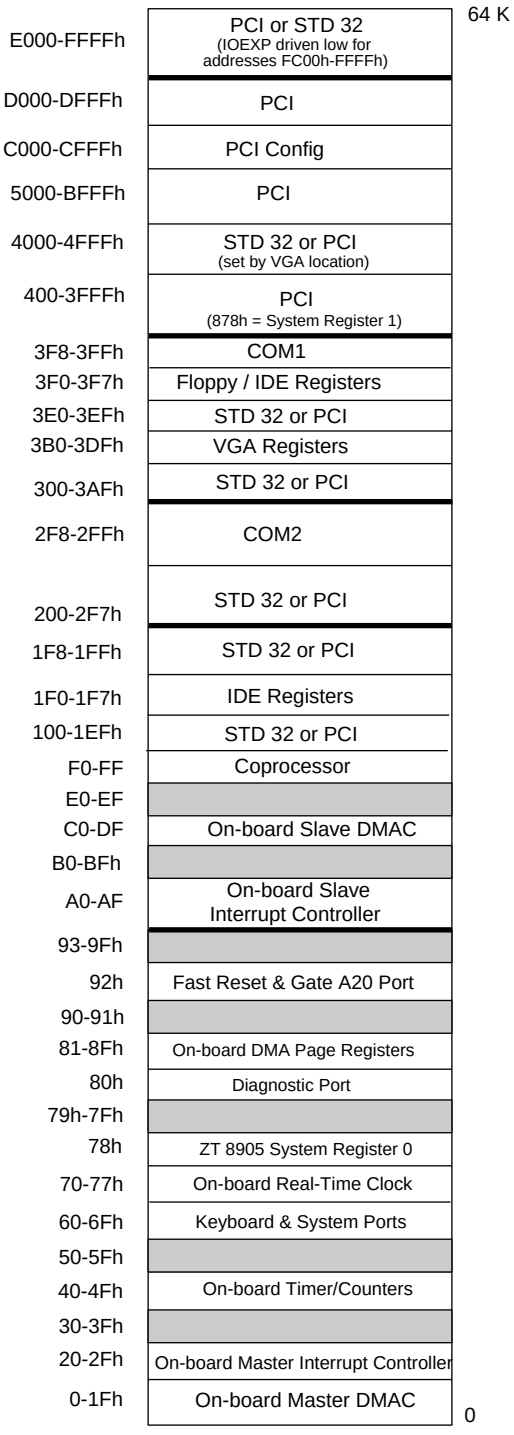
The ZT 8905 addresses up to 64 Kbytes of I/O using a 16-bit I/O address. The address space is divided between I/O local to the board and I/O on the STD bus. Any I/O space not occupied by a local I/O device or STD bus is available for PCI bus expansion. The I/O address regions available for the STD bus are configured through the BIOS SETUP utility (discussed in the section "ZT 8905 SETUP" later in this chapter). During local I/O operations, the STD bus is held static to decrease system electrical noise and power consumption.

STD bus I/O is supported through either Standard Architecture (SA8 or SA16) transfers, or Extended Architecture (EA8, EA16, or EA32) transfers. The ZT 8905 supports the STD bus wait request signal, WAITRQ*, to interface to I/O boards with longer access time requirements than those defined by the STD-80 and STD 32 specifications. The signal EXRDY is supported for EA peripherals that require additional transfer time.

The STD bus I/O expansion signal, IOEXP, is also supported. The IOEXP signal is automatically driven low over the I/O address range FC00h to FFFFh. Application software should use this address range to access STD bus I/O boards decoding IOEXP and fewer than 16 bits of address to prevent the board from being redundantly mapped throughout the 64 Kbyte I/O address space.

The ZT 8905 is populated with many of the most commonly used I/O peripheral devices for industrial control and computing applications. The I/O address location for each of the peripherals is shown in the "I/O Address Map" illustration on the following page.

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8905F02-02

I/O Address Map

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CONNECTOR CONFIGURATION

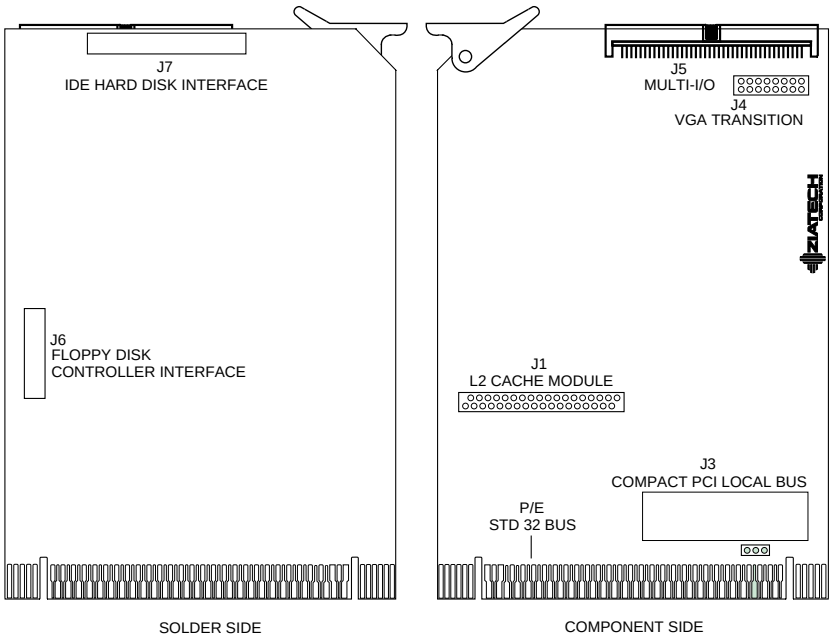
As shown in the "Connector Locations" drawing below, the ZT 8905 includes several connectors to interface to application-specific devices. A brief description of each connector is given in the "Connector Assignments" table below.

Please note the revision of the ZT 8905 that you are using. The table below is for boards that are Revision A and higher, which have different connector assignments than the Revision 0 board. Customers with Revision 0 boards should refer to the Revision 0 manual for connector and cabling information.

Connector Assignments

ZT 8905 Boards Revision A and Higher

Connector	Function
J1	Optional L2 cache module
J2	Fan Connector Location
J3	PCI local bus interface
J4	VGA transition connector
J5	Multi-I/O connector including DMA, Interrupts
J6	Floppy disk controller interface (OEM Option)
J7	IDE hard disk interface

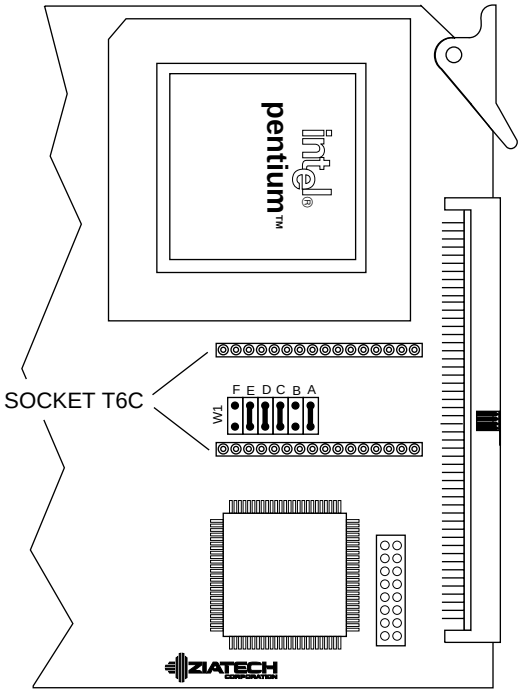


Connector Locations

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JUMPER DESCRIPTIONS

The ZT 8905 includes a few jumper options for features that cannot be provided for through the SETUP utility. As shown in the "Socket T6C Location" figure below, the jumpers are all located underneath the EPROM/FLASH socket (this is the socket used for the alternate boot image). Note that this socket is not normally occupied, allowing the jumpers to be easily accessed. Refer to Appendix A, "Board Configuration," for details.



ZT8905F3-06

Socket T6C Location

ZT 8905 SETUP

The ZT 8905 has many features that can be configured with the BIOS SETUP utility. The SETUP utility is executed during the boot sequence when the **"s"** key is typed. In DOS systems, SETUP may be executed by running the SETUP.COM program from the command line.

The BIOS SETUP utility on all Ziatech CPUs allows configuration of options such as base memory and extended memory size selection, boot source, hard disk type, and floppy disk type. On the ZT 8905, the BIOS SETUP also allows routing of interrupts, memory mapping, and I/O mapping for the STD 32 bus. Previous generation CPU products required jumpers to configure these options. This change makes configuration both faster and more intuitive. PCI peripherals are also automatically configured through the BIOS.

The following topics present an introduction to the setup and configuration of the ZT 8905.

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System Configuration Overview

The Ziatech Industrial BIOS and MS-DOS operating system software is preprogrammed in the ZT 8905's on-board Flash memory. The BIOS includes embedded support to allow the ZT 8905 Flash memory to be used as a solid-state drive (SSD) in the MS-DOS environment. Ziatech also supplies SSD support for other popular operating systems such as Windows NT and QNX (contact Ziatech for SSD drivers for specific operating systems).

The ZT 8905 is configured during the boot sequence by the BIOS. The BIOS uses system configuration information stored as SETUP parameters.

To access the SETUP utility, either boot the system and press the "**s**" key during the system RAM check or, run the SETUP.COM utility from the MS-DOS prompt.

The SETUP parameters are saved in the battery-backed RAM portion of the ZT 8905's real-time clock device.The SETUP parameters can also be saved in a file format, or as the programmed BIOS defaults.

BIOS SETUP Screens

The BIOS SETUP utility for the ZT 8905 is organized as two screens, listed below. †

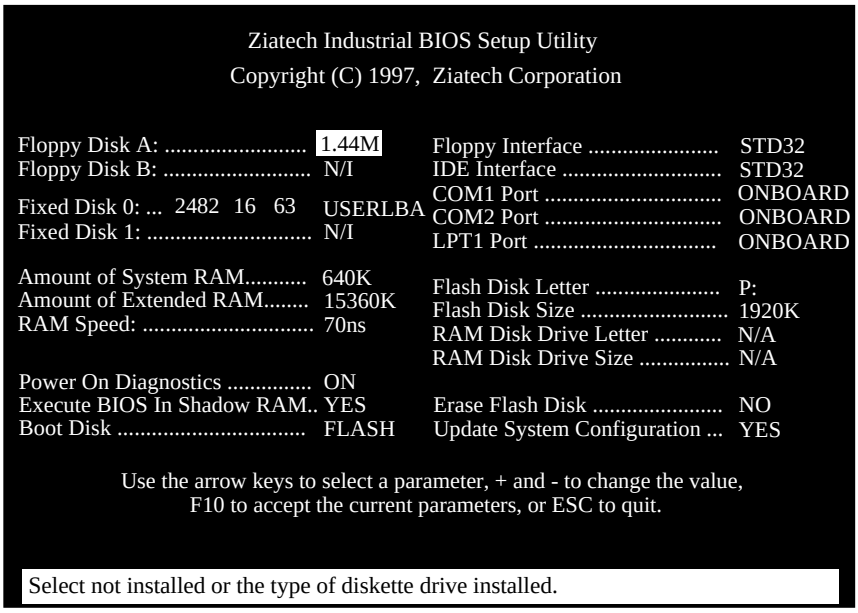
- Screen 1: **Generic option list.** Screen 1 lists the options shared among all Ziatech CPUs. Base memory and extended memory size selection, boot source, hard disk type, and floppy disk type are configurable through this screen.

- Screen 2: **ZT 8905-specific SETUP options.** Options such as interrupt routing and STD 32 memory and I/O addressing are configurable through this screen. Screen 2 is detailed in the section "ZT 8905-Specific SETUP Options" in Appendix A.

† A third screen for STAR SYSTEM configuration options is available when running SETUP on permanent master CPUs. Refer to the *STD 32 STAR SYSTEM User's Manual* for more information.

The parameters in the SETUP screens are easily changed. Use the arrow keys to select a parameter, then press + or - to step through the valid choices for that parameter. A dynamic help line at the bottom of the screens helps you determine how to set each parameter. SETUP accepts only valid parameter sets: if changing one parameter invalidates another parameter, SETUP automatically updates the invalid parameter. After setting the parameters, press the F10 key to accept them. Press the Page Down and Page Up keys to switch between SETUP screens.

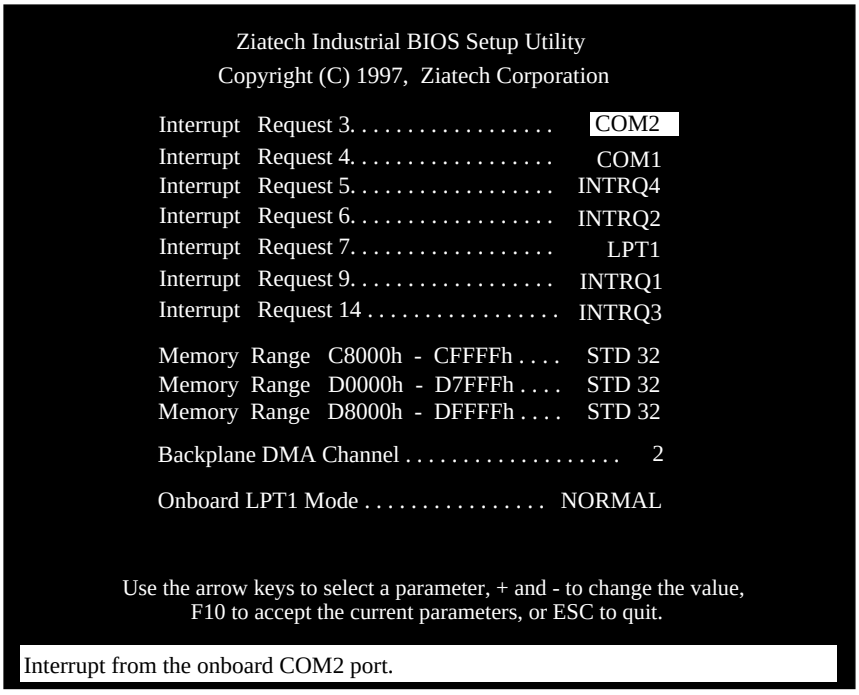
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ZT8905F02-05

BIOS SETUP Utility: Screen 1

Generic SETUP Options



BIOS SETUP Utility: Screen 2

ZT 8905-Specific SETUP Options

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Operating System Installation

It may be necessary to install an operating system such as Windows NT or QNX on the ZT 8905 system. This section describes the generic OS installation process. For OS-specific information, refer to the documentation provided by the OS vendor.

Note: if the installation requires a CD-ROM drive, the appropriate drivers must first be installed in order to access the CD-ROM drive.

1. Use screen 1 in the BIOS SETUP utility to configure the appropriate peripheral devices. Note that the Fixed Disk parameters (used for EIDE drives) include an "AUTO" setting which will cause SETUP to query the drive to determine the correct geometry (cylinders/heads/sectors).

2. Select the proper boot source in the SETUP utility depending on the OS installation media that will be used. For example, if the OS includes a bootable installation floppy, select "FLOPPY" for "Boot Disk" and reboot the system with the installation floppy installed in the floppy drive.

3. Proceed with the OS installation as directed, being sure to select appropriate device types if prompted. See the "ZT 8905 On-Board Device PCI Bus Mapping" table in Appendix D for a list of the PCI devices used on the ZT 8905.

4. When installation is complete, the system should be rebooted and the SETUP "Boot Disk" parameter should be set for the appropriate boot media.

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CHAPTER 3. STD 32 BUS INTERFACE

The ZT 8905 includes several I/O devices common to industrial control applications. The ZT 8905 also operates with the STD 32 bus architecture to support additional I/O and memory mapped devices as required by the application. This chapter discusses the STD 32 architecture and its effect on the operation of the ZT 8905.

STD 32 BACKGROUND

The *STD-80 Series Bus Specification*, developed in the early 1980s by Ziatech Corporation, defines the electrical, mechanical, and functional characteristics of an STD bus system based on the 8088 series of microprocessors. Features of an STD-80 system include an 8-bit data bus, 24-bit address bus, and single bus master operation.

In the late 1980s, Ziatech developed the *STD 32 Bus Specification and Designer's Guide* as an extension to the *STD-80 Series Bus Specification*. Features of an STD 32 system include compatibility with STD-80 memory and I/O boards, expansion capabilities of up to a 32-bit data bus and a 32-bit address bus, and support for multiple bus master operation.

STD-80 PERIPHERAL SUPPORT

The ZT 8905 is electrically compatible with Revision 2.3 of the *STD-80 Series Bus Specification* (Ziatech part number ZT MSTD80), allowing peripherals that were designed for that specification to be used with the ZT 8905 in an STD 32 backplane. The ZT 8905 cannot be used in an STD-80 backplane because of the additional signals needed for EA 32-bit addressing. However, STD-80 boards can be used with the ZT 8905 in an STD 32 backplane. STD-80 superset features supported by the ZT 8905 include:

- A 24-bit address bus
- Four additional maskable interrupts
- Dynamically driven I/O expansion
- DMA slave support

The following topics discuss these features.

Address Multiplexing

The *STD-80 Series Bus Specification* defines a multiplexing scheme to transfer address lines A16 through A19 across the lower half of the data bus during the start of each memory cycle. The ZT 8905 extends this concept by also transferring address lines A20 through A23 across the upper half of the data bus.

This feature is especially useful if all memory mapped STD bus boards used in the system decode 24 bits of address. If a memory mapped board decodes fewer than 24 bits, the board appears multiple times in the 24-bit memory map.

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Interrupts

The *STD-80 Series Bus Specification* defines a single interrupt signal, INTRQ* (P44). If STD bus maskable interrupts are used in the application, the ZT 8905 is configurable to receive INTRQ* and four optional interrupts: INTRQ1* (P37), INTRQ2* (P50), INTRQ3* (E67), and INTRQ4* (P6). STD bus peripheral boards must be capable of generating an interrupt on INTRQ1*, INTRQ2*, INTRQ3*, and INTRQ4* to use this feature.

I/O Expansion

The *STD-80 Series Bus Specification* defines an I/O expansion signal, IOEXP, used to reduce addressing redundancy of an I/O board decoding fewer than 16 address lines. The ZT 8905 automatically drives this signal low when the application software performs an STD bus I/O address in the address range FC00h through FFFFh. To use this feature:

- The I/O mapped STD bus board is configured to respond to an active low IOEXP.
- The application software assigns the board to address FC00h plus the board configuration offset.

DMA Slave Support

The ZT 8905 supports DMA slaves through either backplane or frontplane signaling. The STD 32 specification defines control signals for backplane DMA transfers to peripherals such as the ZT 8954 Floppy Disk Interface. The ZT 8905 supports up to three DMA slaves controlled via a 10-pin frontplane header provided by the ZT 90205 cable.

STD 32 BUS COMPATIBILITY

The ZT 8905 is compatible with the *STD 32 Bus Specification and Designer's Guide* (Ziatech part number ZT MSTD32). The STD 32 bus allows both older STD-80 style peripherals and new higher performance peripherals as defined by STD 32 to be used in the same backplane. STD 32 separates older peripherals and newer peripherals into Standard Architecture, Extended Architecture, and Multiprocessing, as described in the following topics.

Standard Architecture

Standard Architecture 8- and 16- bit peripherals are referred to as SA8 and SA16, respectively. The ZT 8905 supports interfacing to both SA8 and SA16 peripherals. Older STD-80 style peripherals are compatible with SA8 transfers, allowing the ZT 8905 to support these peripherals. The ZT 8905 automatically determines the type of transfer at the start of each STD bus operation. If the application software includes a 16-bit operation with an 8-bit STD bus (SA8) board, the ZT 8905 automatically reduces the transfer into two STD bus cycles. If the application software includes a 16-bit operation with a 16-bit STD 32 (SA16) board, the ZT 8905 performs the transfer in a single STD bus cycle. A single STD cycle for SA peripherals is typically seven STD 32 clock periods.

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Extended Architecture

Extended Architecture 8-, 16-, and 32-bit peripherals are referred to as EA8, EA16, and EA32, respectively. The ZT 8905 supports interfacing to all three data width types. The ZT 8905 dynamically senses the type of peripheral at the start of the backplane cycle and will scale the transfer to match the data width of the peripheral. The memory addressing for EA peripherals is 32 bits (4 Gbytes); I/O addressing is 16 bits (64 Kbytes). EA cycles are typically completed in three STD 32 clock periods.

Multiprocessing

In addition to the different data transfer modes, the STD 32 system has another advantage: it supports up to seven processor boards in a single system. With the addition of an STD bus arbiter, such as the ZT 89CT39, multiple ZT 8905 boards have fixed or rotating priority access to STD bus memory and I/O resources. This architecture is useful for applications that can be divided into modular control blocks, with each module running on a unique ZT 8905. Ziatech manufactures several boards that are compatible with the multiprocessing architecture.

STD 32 Compliance Levels

STD 32 features are discussed in terms of compliance levels. The compliance codes can be used to determine the general capabilities of a board, particularly when configuring a system composed of boards from different manufacturers.

Permanent Master: EA32, EA16, EA8, SA16, SA8-{MD}, I, SDMA8, SDMA16, SDMABP

Temporary Master: SA16, SA8-{MX}, I, SDMA8, SDMA16, SDMABP

The following are brief descriptions of the STD 32 compliance levels supported by the ZT 8905.

EA8, EA16, EA32 Supports 8-bit, 16- and 32-bit data transfers with STD 32 Extended Architecture signal format and timings. The ZT 8905 automatically determines the width of the data transfer at the start of each STD bus operation. Memory addresses are 32 bits wide (4 Gbytes), and I/O addresses are 16 bits wide (64 Kbytes).

SA8, SA16 Supports 8-bit and 16-bit data transfers with STD-80 signal format and timings. The ZT 8905 automatically determines the width of the data transfer at the start of each STD bus operation. STD-80 compatible memory and I/O boards are supported.

I Supports four additional STD bus interrupts: INTRQ1*, INTRQ2*, INTRQ3*, and INTRQ4*. These interrupts are input from the STD bus and connected to the interrupt controller through a software configurable switch. This feature is supported by the BIOS SETUP program.

{MX} Supports the multiple master (MREQx*, MAKx*) protocol. These two signals are used by the ZT 8905 in a multiple master architecture to gain control of STD bus resources. The use of these signals requires a bus arbiter, such as the ZT 89CT39, to be plugged into Slot X. The ZT 8905 requires Revision D or higher of the ZT 89CT39.

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SDMA16, SDMA8 Supports 8-bit or 16-bit Standard Architecture DMA as defined in the *STD 32 Bus Specification and Designer's Guide*. Control signals are provided through the frontplane connector.

SDMABP Supports Standard Architecture DMA using BUSRQ*/BUSAK* for request and acknowledge and the backplane DMA control signals DMAIOR*, DMAIOW*, and T-C.

STD BUS INTERRUPTS

The ZT 8905 supports both maskable and non-maskable interrupts from the STD bus. This section discusses system level issues related to these interrupts. Refer to Chapter 4, "Interrupt Controller" for more information on the maskable interrupt controllers.

Maskable Interrupts

The STD bus maskable interrupts monitored by the ZT 8905 are INTRQ* (P44), INTRQ1* (P37), INTRQ2* (P50), INTRQ3* (E67), and INTRQ4* (P6). These maskable interrupts are configurable through the BIOS SETUP mechanism.

The ZT 8905 is also capable of generating STD bus or frontplane interrupts. This feature is useful in multiple master systems to coordinate communications between processors. Typically, INTRQ4* is used for this feature in STD 32 STAR SYSTEMs.

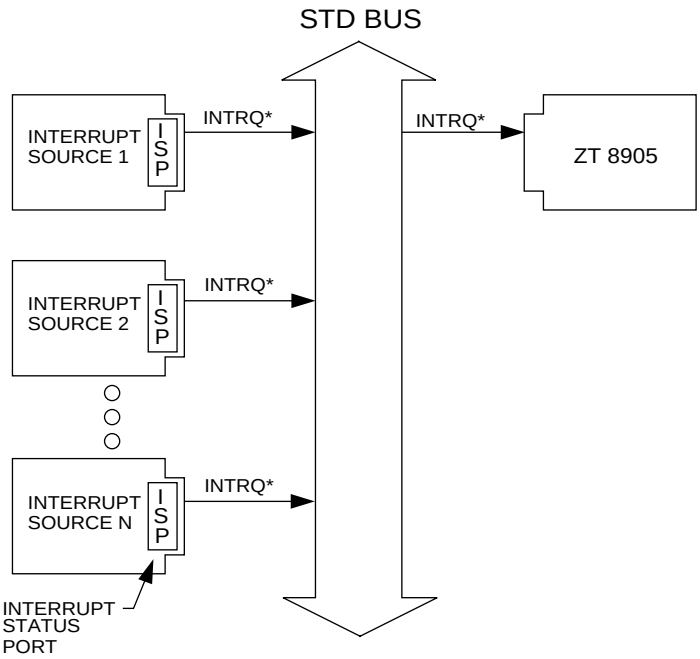
Some applications may find it necessary to share multiple interrupt sources on a single STD bus interrupt request, as shown on the following page in the "STD Bus Polled Interrupt Structure" illustration. Since the interrupt controller provides a single vector for each input, it is up to the application software to poll each possible source on the shared interrupt request signal to determine which is requesting service. This procedure is fine for most applications, provided that each source can be polled and that the interrupt controller is programmed for level-triggered operation.

Some applications include edge-triggered interrupt sources. For example, the Ziatech DOS System uses edge-triggered interrupts to support the timer used to generate the periodic system tick. Normally, the 8259 interrupt controller inputs are not independently programmable for edge-triggered or level-triggered interrupts, all inputs for these applications must be treated as edge-triggered. The ZT 8905 uses an enhanced version of the 8259 interrupt controller which does allow individual interrupt levels to be configured.

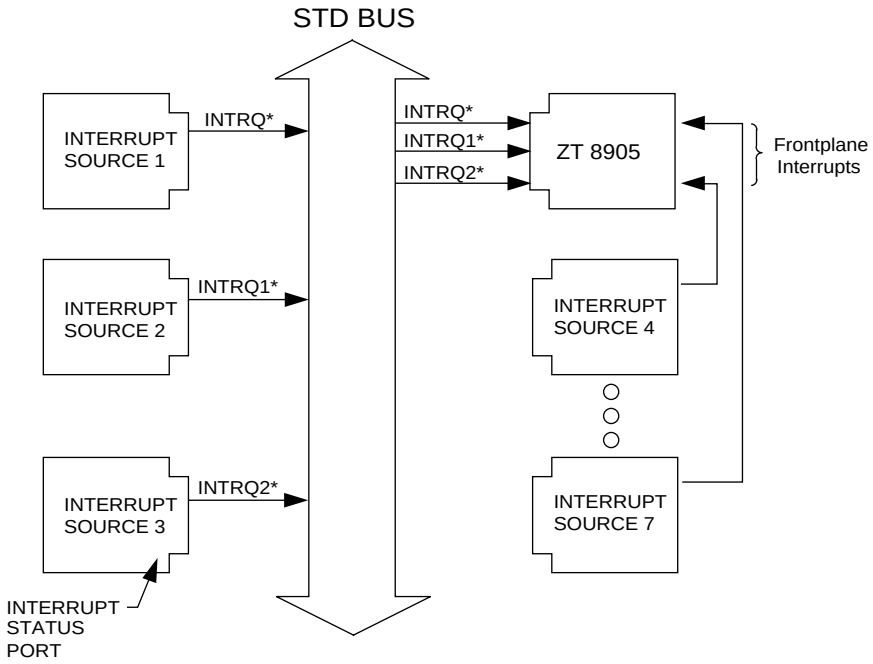
In an edge-triggered architecture, multiple interrupt sources should not share the same interrupt request signal because it is possible to miss an interrupt request from one source while an interrupt request from another source is being serviced. For this architecture, each interrupt source requires a unique connection to the interrupt controller, as shown in the "STD Bus Vectored Interrupt Structure" illustration on the following page.

The ZT 8905 can have up to 10 independent interrupt sources from off-board devices (5 from the backplane, 5 from the frontplane). Note that normally, some of the available interrupt controller inputs are reserved for on-board use, which may limit availability for off-board peripherals. For example, if the on-board COM ports are being used, then IR3 and IR4 are not available for off-board use.

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STD Bus Polled Interrupt Structure

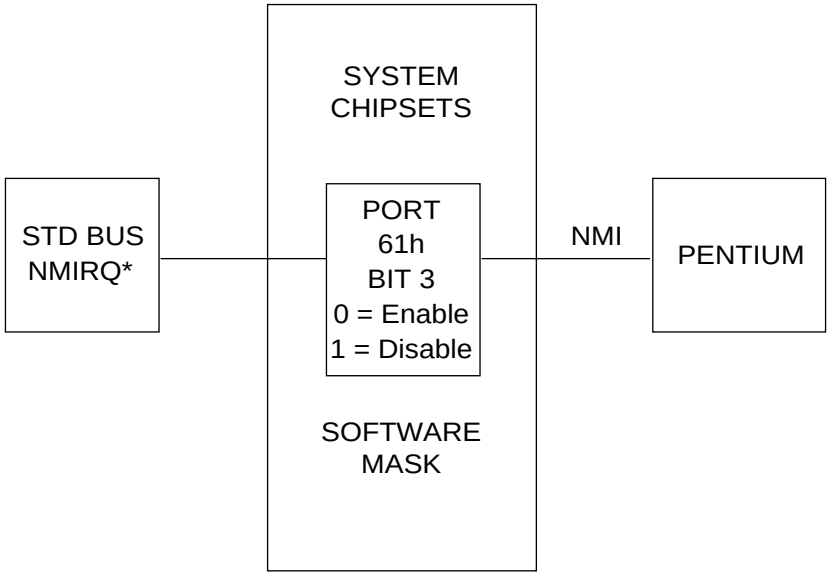


STD Bus Vectored Interrupt Structure

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Non-Maskable Interrupts

The ZT 8905 supports the STD 32 signal NMIRQ* for system errors (see the "Non-Maskable Interrupt Structure" illustration below). The NMIRQ* signal is maskable through port 61h, bit 3. Write a 0 to enable, or a 1 to disable HMI for bit 3 of port 61h.



Non-Maskable Interrupt Structure

RESET

The ZT 8905 is automatically reset with a precision voltage monitoring circuit that detects when Vcc is below the acceptable operating limit of 4.75 V. In addition, the on-board 3.3 V power supply is monitored and will reset the ZT 8905 when below 3.0 V. Other sources of reset include the watchdog timer, local pushbutton switch, and the STD bus pushbutton reset signal, PBRESET* (P48).

The ZT 8905 responds to any of these reset sources by initializing local peripherals and driving the STD bus system reset, SYSRESET* (P47). Refer to the section on "Multiple Master Reset" in this chapter for further details about that environment.

MULTIPLE MASTER AND INTELLIGENT I/O

Ziatech offers two architectures for increasing the number of microprocessors in a single system: multiple master and intelligent I/O. Applications can use multiple master, intelligent I/O, or a combination of the two.

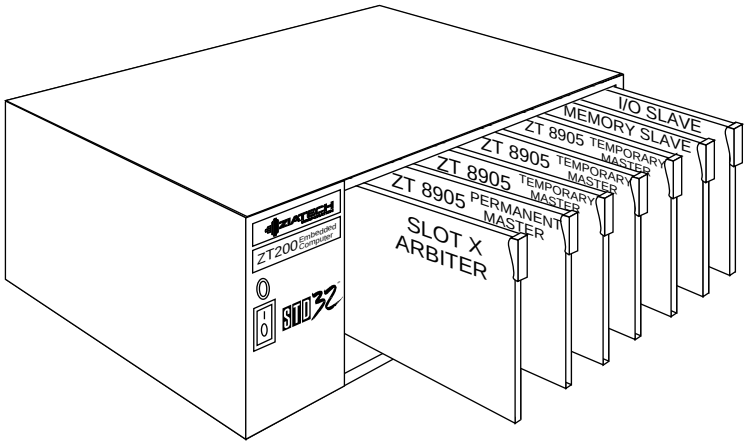
The following topics discuss multiple master, intelligent I/O, multiple master vs. intelligent I/O, multiple master system requirements, and reset.

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Multiple Master

A multiple master architecture requires one permanent master and one or more temporary masters, as illustrated in the "Multiple Master Architecture" figure below. The ZT 8905 is configurable for either permanent or temporary master operation. Each master has complete access to STD bus resources and operates at full speed when the local CPU is communicating with local memory and I/O. It is not until the application software attempts an STD bus access that arbitration occurs.

The ZT 8905 responds to an STD bus access from the application software by generating an STD bus request, MREQx* (E70), to an external bus arbiter, such as the ZT 89CT39. The ZT 89CT39 must be Revision D or higher. The ZT 8905 then suspends all local operation until the bus arbiter returns an STD bus acknowledge, MAKx* (E69). All arbitration is done in hardware on the external bus arbiter board and is transparent to the application software. The amount of time required for this arbitration depends on the amount of time higher priority masters are in control of STD bus resources. A shared resource locking mechanism is supported to guarantee exclusive access to STD bus memory or I/O.



Multiple Master Architecture

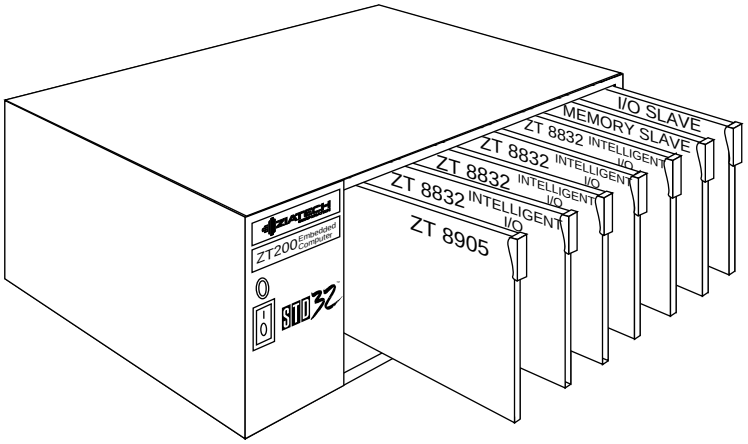
Intelligent I/O

An intelligent I/O system includes a single ZT 8905 and one or more intelligent I/O boards, such as the ZT 8832. This architecture is illustrated in the "Intelligent I/O Architecture" figure on the following page. The intelligent I/O board incorporates several I/O devices, a dual-port RAM for processor communications, and a CPU dedicated to controlling these devices.

Each intelligent I/O board operates at full speed when communicating with local memory, local I/O, and dual-port RAM. The ZT 8905 also operates at full STD bus speeds when accessing the dual-port RAM. It is not until the ZT 8905 and the intelligent I/O board access the dual-port RAM at the same time that arbitration occurs.

All arbitration is done in hardware local to each intelligent I/O board, eliminating the need for an external bus arbiter. The arbitration is transparent to the application software. The amount of time required for arbitration depends on the amount of time the device in control of the dual-port RAM requires to complete operation. A shared resource locking mechanism is supported to guarantee exclusive access to dual-port RAM by either the ZT 8905 or the intelligent I/O board.

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Intelligent I/O Architecture

Multiple Master Vs. Intelligent I/O

Both multiple master and intelligent I/O architectures are excellent methods of increasing system performance. The application designer has the freedom to select either architecture or combine both to meet the needs of the specific application. The following is a brief comparison of the multiple master and intelligent I/O architectures.

- An advantage of the multiple master system is that each ZT 8905 has complete access to all STD bus memory and I/O resources. In an intelligent I/O system, only the ZT 8905 has access to STD bus memory and I/O, including the dual-port RAM interface to each intelligent I/O board.

- An advantage of the intelligent I/O system is lower system cost. The intelligent I/O architecture operates in both STD-80 and STD 32 bus structures. Dual port RAM arbitration is local to each intelligent I/O board, eliminating the need for a system arbiter. Also, most multiple master implementations require an STD bus memory slave for communications between the masters. With an intelligent I/O architecture, all communications between the single master and the intelligent I/O boards are through the dual-port RAM local to each intelligent I/O board.

Multiple Master System Requirements

The following is a list of considerations for the ZT 8905 operating in a multiple master architecture.

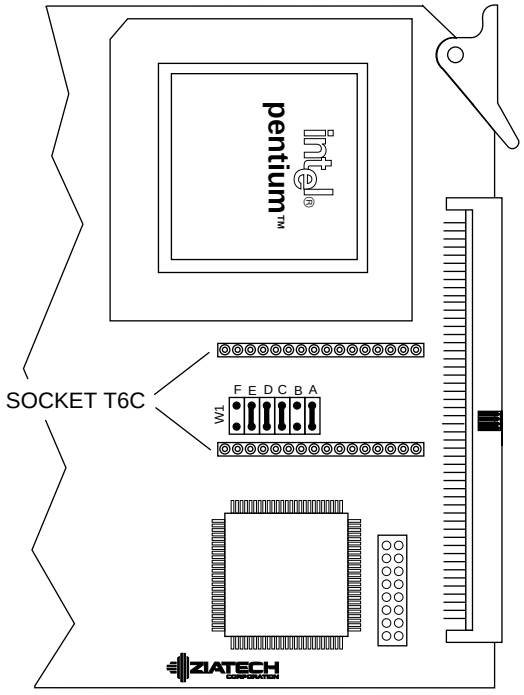
- One ZT 8905 must be configured as a permanent master, or there must be another permanent master in the system. The permanent master is responsible for managing the STD bus clock, CLOCK* (P49), and the system reset, SYSRESET (P47). The remaining ZT 8905 boards must be configured for temporary master operation.

  To configure the ZT 8905 for permanent or temporary mode, RP2 and RP3 are used. Installing these resistor packs configures the ZT 8905 for permanent master operation (the default); removing them will configure the ZT 8905 for temporary master operation. These resistor packs are located near the STD 32 gold fingers. RP2 and RP3 also provide pullup resistors for the SA open collector signals on the STD 32 backplane. As there can only be one master that provides the pullup mechanism, it is logical to always have the permanent master provide this feature. RP1

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is also used to pull up the EA control signals that are open collector. Only one master in the system can provide these pullups. Normally, RP1 will be removed when configured as a temporary master (RP2 and RP3 removed). If another CPU type that is SA only (for example, ZT 8901, ZT 8902, ZT 8903, ZT 8904) is configured as a permanent master, then one ZT 8905 must have RP1 installed to provide the pull-up feature for the STD 32 backplane. If two or more ZT 8905s are being used as temporary masters to one 16-bit board (e.g. ZT 8902), then only one of the ZT 8905 temporary masters can have RP1 installed.

- An STD 32 backplane is required.
- A ZT 89CT39, ZT 8911 (CPU/arbiter), or equivalent bus arbiter is needed to manage ZT 8905 access to the STD bus resources. If the ZT 89CT39 is used, it must be Revision D or higher.
- If a local PCI VGA interface is not used in multiple master operation and an STD 32 shared VGA is used, a ZT 96048 emulation RAM must be loaded in socket T6C (shown below) to retain video memory when the ZT 8905 is switched away from the backplane VGA device.



ZT8905F3-06

Socket T6C Location

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Multiple Master Reset

In a multiple master system, a ZT 8905 configured as a permanent master operates the same as a ZT 8905 operating in a single master architecture. The permanent master monitors Vcc with a precision voltage monitoring circuit and holds the system in reset when Vcc is below 4.75 V. The permanent master also will hold the system in reset when either the on-board pushbutton reset is asserted or the STD 32 bus signal PBRESET* (P48) is asserted. The permanent master asserts SYSRESET* (P47) to hold the system in reset.

A ZT 8905 configured as a temporary master manages reset differently. A temporary master does not monitor PBRESET* and does not generate SYSRESET*. Instead, a temporary master ignores PBRESET* and monitors SYSRESET*. This enables the temporary masters to be reset when the permanent master generates SYSRESET*. This also enables the pushbutton reset on the temporary master to reset only the temporary master while the pushbutton on the permanent master resets the entire system.

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CHAPTER 4. INTERRUPT CONTROLLER

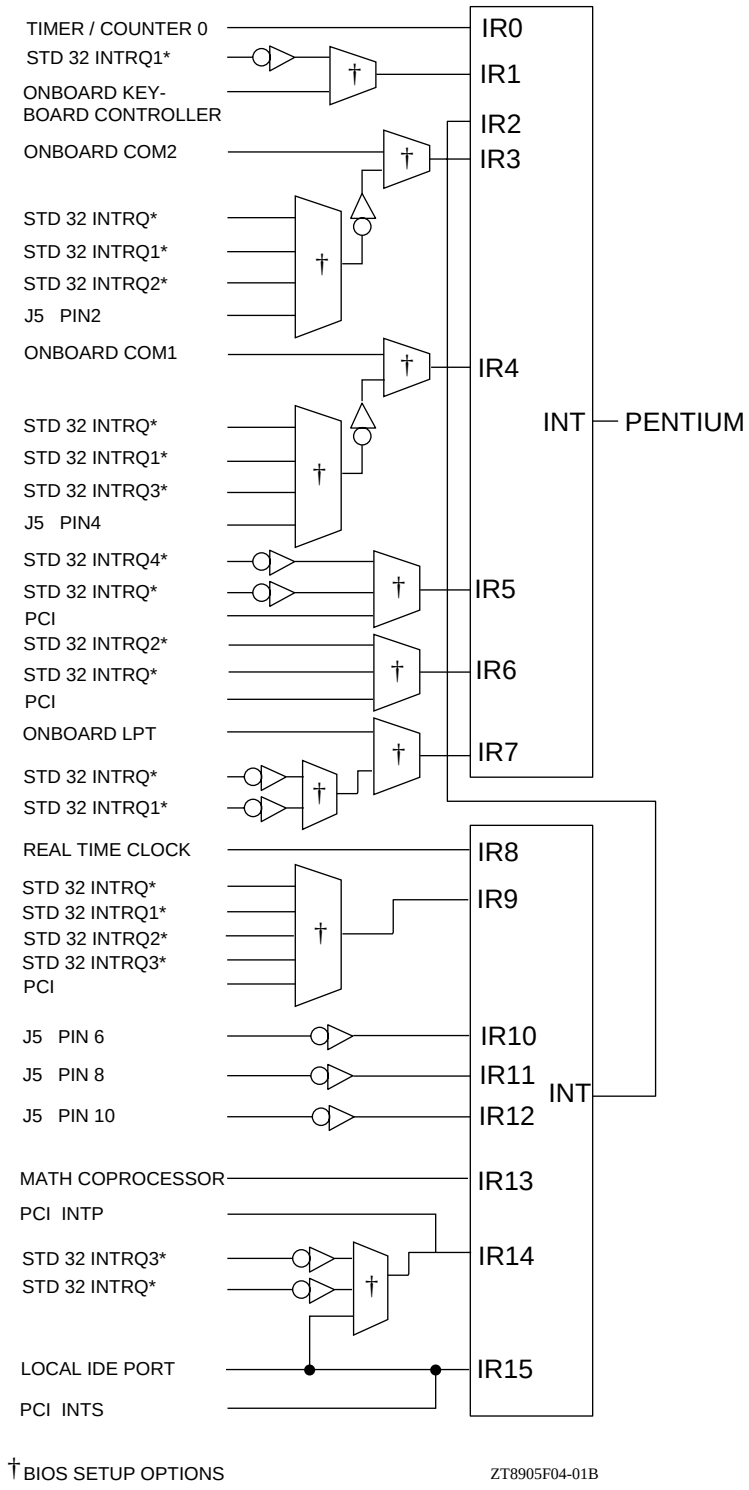
The ZT 8905 includes two Intel-compatible 8259 cascaded interrupt controllers that provide a programmable interface between interrupt-generating peripherals and the CPU. The interrupt controllers monitor 15 interrupts with programmable priority. When peripherals request service, the interrupt controller interrupts the CPU with a pointer to a service routine for the highest priority device.

The major features of the interrupt architecture are listed below. The ZT 8905 does not support cascaded interrupt controllers on the STD bus or slot-specific interrupts.

- 15 individually maskable interrupts
- Jumperless configuration
- Level-triggered or edge-triggered recognition
- Fixed or rotating priorities
- PCI Interrupt support
- PCI Extended Mode register support

The interrupt architecture is illustrated in the "Interrupt Architecture" figure on the following page. Interrupt configuration is performed through screen 2 of the BIOS SETUP utility (discussed in Appendix A) and allows the user to set up the interrupt architecture to the needs of the application. The SETUP utility allows most of the interrupt controller interrupts to be configured from a variety of interrupt sources. The ZT 8905 supports the Extended Mode register, which allows individual programming of low-level triggered or active high-edge triggered interrupts.

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Interrupt Architecture

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INTERRUPT SOURCES

The interrupt sources are summarized below.

Backplane: There are five STD bus interrupts routed to the interrupt configuration selection logic: INTRQ*, INTRQ1*, INTRQ2*, INTRQ3*, and INTRQ4*. These interrupts are active-low on the STD bus and inverted before they reach the interrupt configuration logic.

Frontplane: Two of the five frontplane interrupts are routed to the interrupt configuration logic. These interrupts are available through the multi-I/O connector J5 as active-low inputs that are inverted before reaching the interrupt configuration logic. The remaining three frontplane interrupts are directly tied to the interrupt controller, after being logically inverted. The pin assignments for connector J5 are given in Appendix B. Many STD bus boards support a 10-pin header connector for routing interrupts to the ZT 8905 through a ribbon cable. This architecture is useful if the application requires more interrupts than are available on the STD bus backplane.

PCI: Four interrupt levels may be assigned to the PCI bus when not used for other devices. IR5, IR6, IR9, and IR14 may be allocated to PCI through screen 2 of the BIOS SETUP utility. For more on the BIOS SETUP utility, see the section "BIOS SETUP Overview" in Appendix A. The PCI configuration utility then assigns interrupts to PCI devices as needed. In STAR SYSTEMs, IR5 is not available for PCI allocation. If an STD 32 floppy disk controller is used, IR6 is not available for PCI use.

Local: Local interrupt sources include the keyboard controller, serial ports (COM1, COM2), multiprocessor communications, 1284 parallel port, real-time clock, timer/counters, DMA controller, Math coprocessor, watchdog timer, and optional IDE controller.

PROGRAMMABLE REGISTERS

Each interrupt controller includes four initialization registers, three control registers, and three status registers. The I/O port addressing for the interrupt controllers is given in the "Interrupt Controller Register Addressing" table below. The base address of the master interrupt controller is 20h and the base address of the slave interrupt controller is A0h.

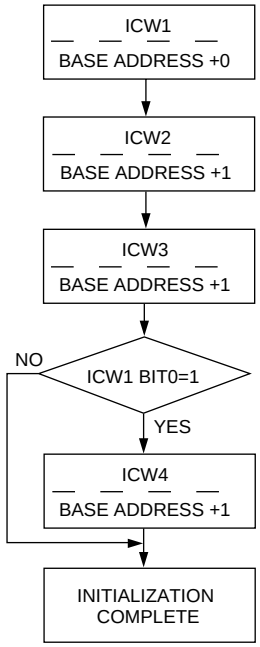
Interrupt Controller Register Addressing

Address	Register	Operation
Base+0h	IRR, ISR, IPR	Read
Base+0h	ICW1	Write
Base+0h	OCW2, OCW3	Write
Base+1h	OCW1	Read/Write
Base+1h	ICW2, ICW3, ICW4	Write

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Initialization Registers (ICW1-ICW4)

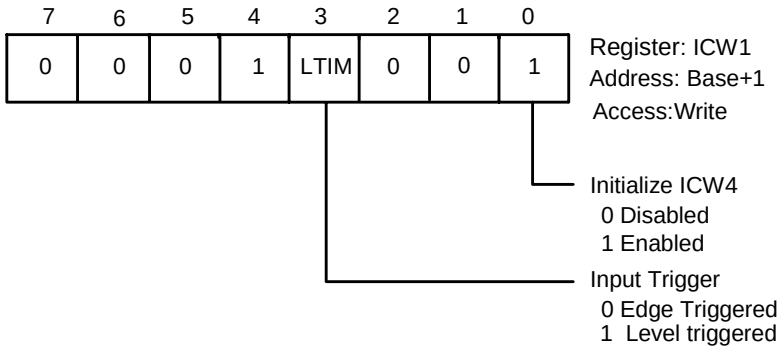
Each interrupt controller must be initialized before it is used. Initialization consists of writing two, three, or four initialization commands. The programming sequence for these registers is given in the "Interrupt Initialization Programming" figure. ICW1, ICW2, and ICW3 must be programmed during each initialization sequence. ICW4 may or may not be programmed, as required by the application.



Interrupt Initialization Programming

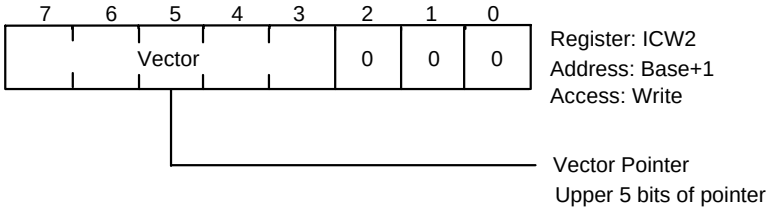
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Initialization Register ICW1



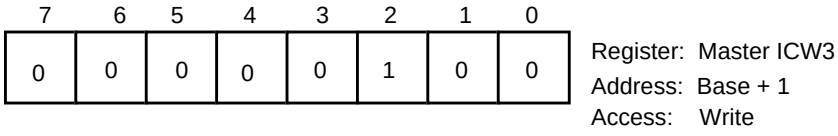
Initialization Register ICW1

Initialization Register ICW2

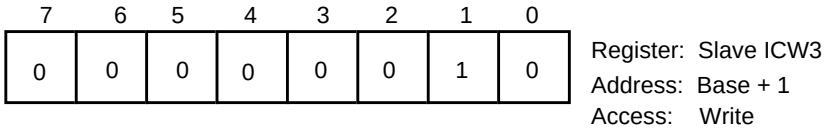


Initialization Register ICW2

Initialization Register ICW3



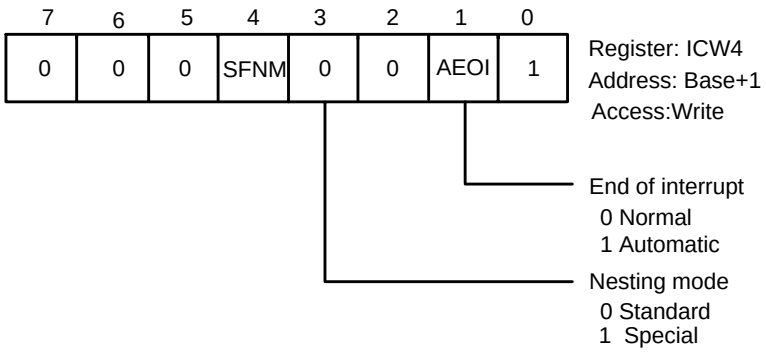
Master Initialization Register ICW3



Slave Initialization Register ICW3

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Initialization Register ICW4

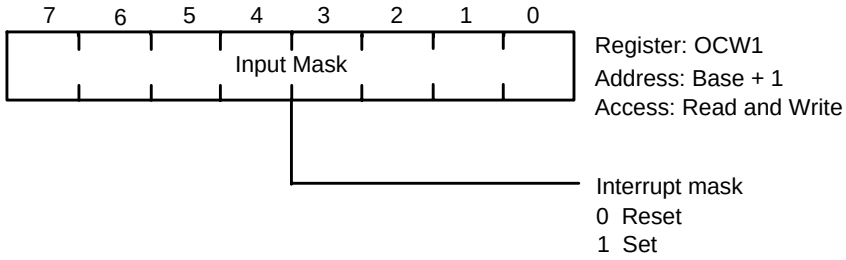


Initialization Register ICW4

Operational Registers (OCW1-OCW3)

The operation of each interrupt controller is managed by three 8-bit operational registers. These registers are programmed in any sequence for things such as enabling and disabling interrupt requests and changing interrupt priorities. Illustrations of the three operational registers are presented in the following topics.

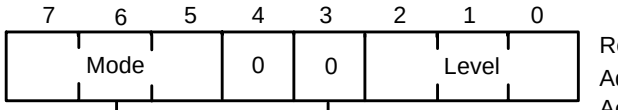
Operational Register OCW1



Operational Register OCW1

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Operational Register OCW2



Register: OCW2
Address: Base + 0
Access: Write

Interrupt level
000 IR0
001 IR1
010 IR2
011 IR3
100 IR4
101 IR5
110 IR6
111 IR7

Operational mode
End of Interrupt
001 Non-specific
011 Specific

Automatic Rotation
101 Rotate on non-specific
100 Rotate on automatic (set)
000 Rotate on automatic (reset)

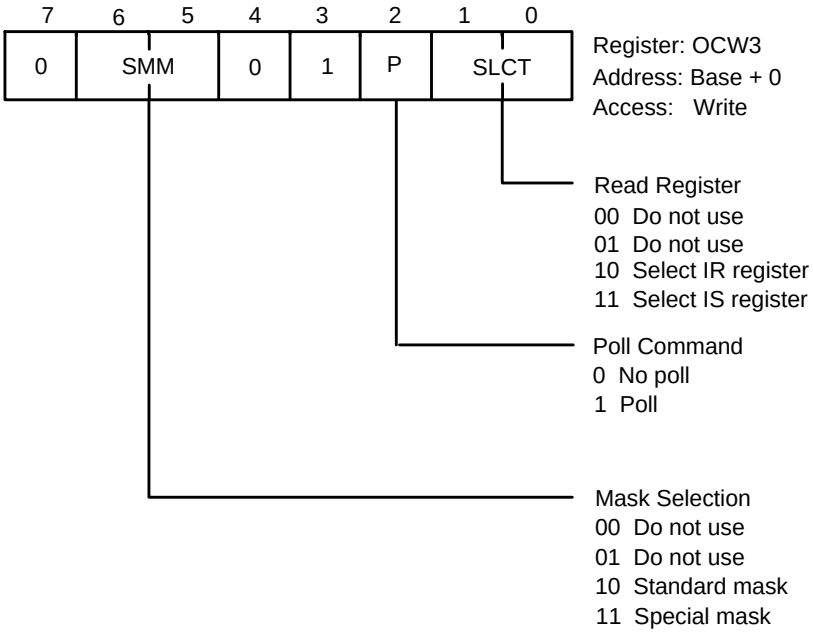
Specific Rotation
111 Rotate on specific
110 Set priority level

No Operation
010 Do not use

Operational Register OCW2

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Operational Register OCW3

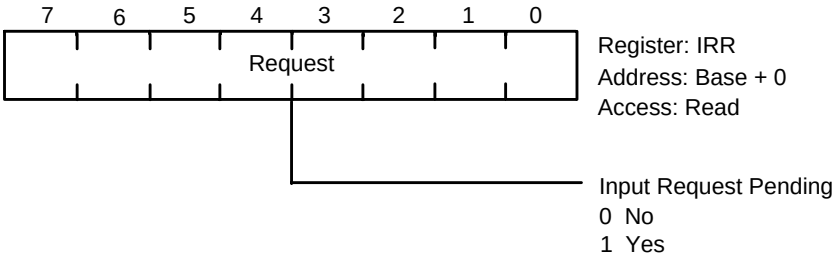


Operational Register OCW3

Status Registers (IRR, ISR, IPR)

Each interrupt controller includes three status registers. A status register is selected by programming the first three bits of OCW3.

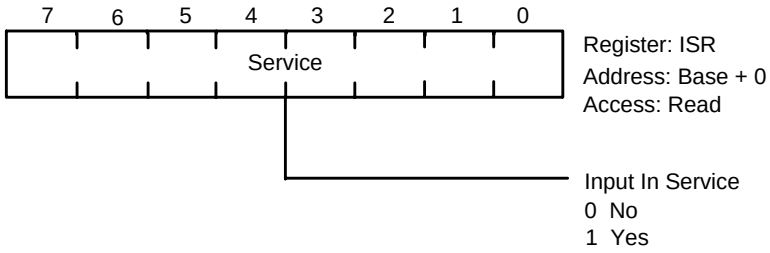
Status Register IRR



Status Register IRR

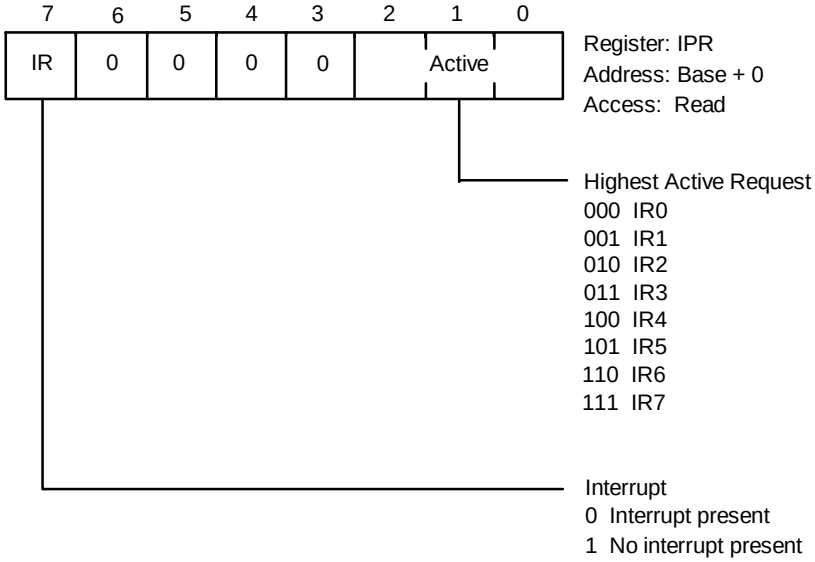
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Status Register ISR



Status Register ISR

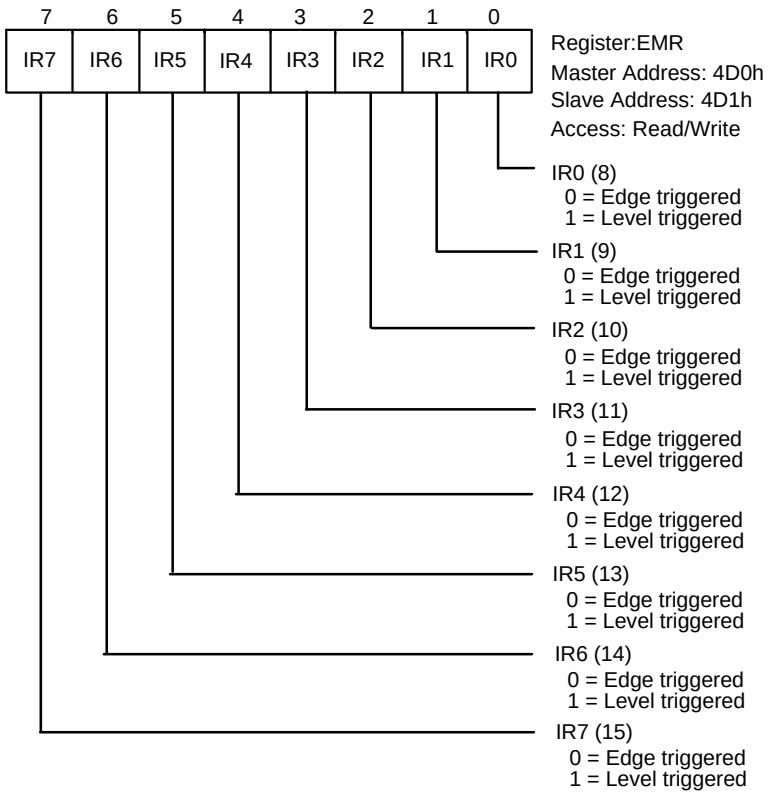
Status Register IPR



Status Register IPR

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Extended Mode Register



Extended Mode Register

ADDITIONAL INFORMATION

Refer to the *Ziatech Industrial Computer System Manual* for more information on the operating system's use of the interrupt inputs. Refer to the Intel *Peripheral Components, 1995* data book for more information on the 8259 interrupt controller operating modes.

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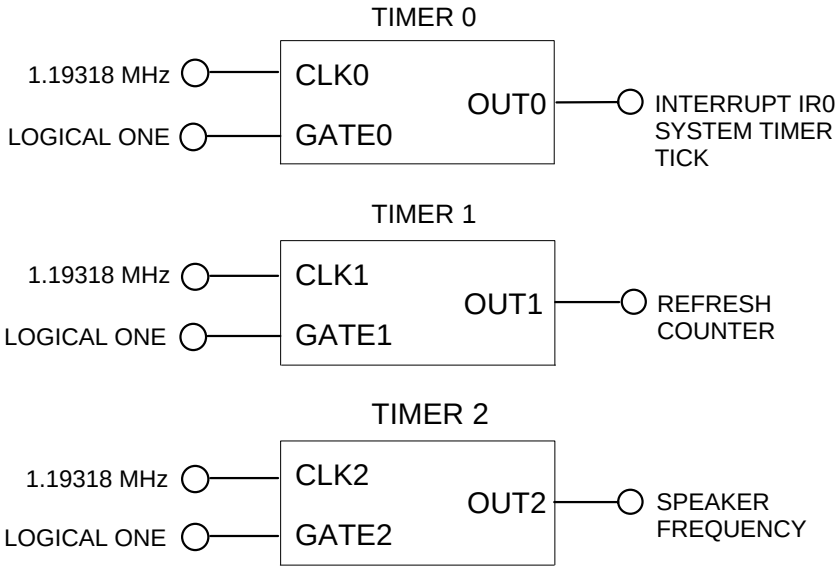
CHAPTER 5. COUNTER/TIMERS

The ZT 8905 includes one Intel-compatible 8254 device with a total of three programmable counter/timers. The counter/timers are useful for software timing loops, timed interrupts, and periodic interrupts. The major features of the counter/timers are listed below.

- Three 16-bit counter/timers
- Six programmable operating modes
- Binary and BCD counting
- Interrupt and polled operation

The counter/timer architecture is illustrated in the "Counter/Timer Architecture" figure below. In some cases, not all counter/timers are available for application development. In an MS DOS system, for example, counter/timer 0 generates a periodic system interrupt and should not be programmed by the application. Please refer to the selected operating system manual for more information.

The six programmable operating modes are summarized in the "Counter/Timer Operating Modes" table on the following page.



Counter/Timer Architecture

Counter/Timer Operating Modes

Mode	Counter/Timer Output Operation
0	Transitions after programmed count expires. Gate tied high to enable counting.
1	Transitions after programmed count expires. Gate tied high to enable counting.
2	Periodic single pulse after programmed count expires. Gate tied high to enable counting
3	Square wave with frequency equal to programmed count. Gate tied high to enable counting.
4	Single pulse after programmed count expires. Gate tied high to enable counting.
5	Single pulse after programmed count expires. Gate tied high to enable counting.

PROGRAMMABLE REGISTERS

The counter/timers are accessed through four I/O addresses, as shown in the "Counter/Timer Register Addressing" table below. Each counter/timer occupies an I/O port address through which the preset count values are written and both the count and status information is read. The Control register occupies the remaining I/O port address, which services all three counter/timers.

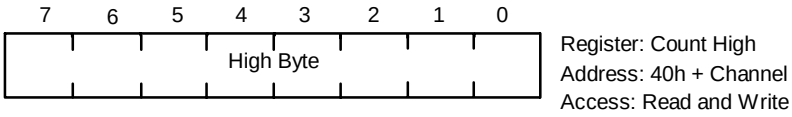
Counter/Timer Register Addressing

Address	Register	Operation
0040h	Channel 0 Count	Read/Write
0040h	Channel 0 Status	Read
0041h	Channel 1 Count	Read/Write
0041h	Channel 1 Status	Read
0042h	Channel 2 Count	Read/Write
0042h	Channel 2 Status	Read
0043h	Control	Write

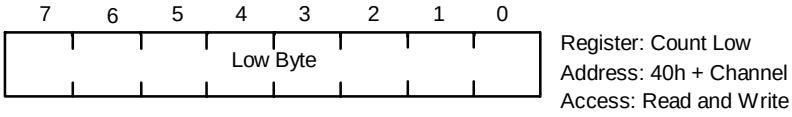
Count Registers and Count Latch

Each counter/timer has a 16-bit Count Register and 16-bit Count Latch Register. The Count Register is programmed with the initial count and is updated according to the mode in which the counter/timer is programmed. The Count Latch Register is used to read the current count. The Access bits in the General Control Register define the method for accessing the 16-bit Count and Count Latch Registers (low byte, high byte, low byte followed by high byte).

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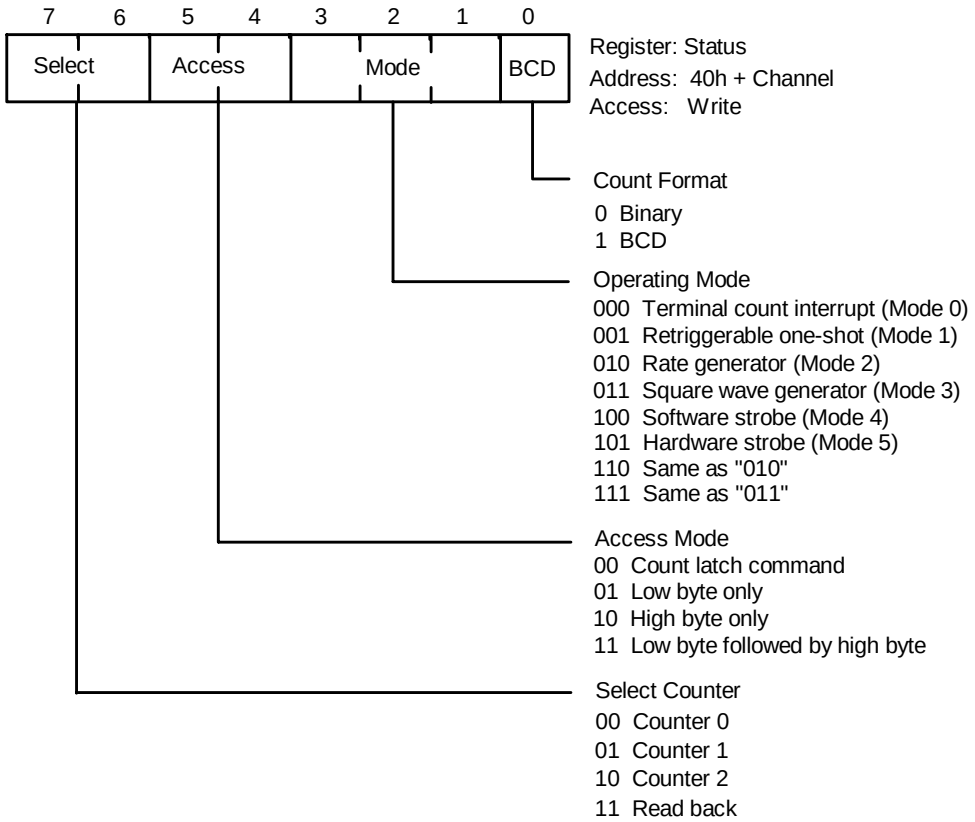
Count Register High Byte



Count Register Low Byte

Status Register

Each counter/timer has a Status Register. The Status Register must be read using the multiple latch command specified in the Multiple Latch Control Register (see end of this chapter).



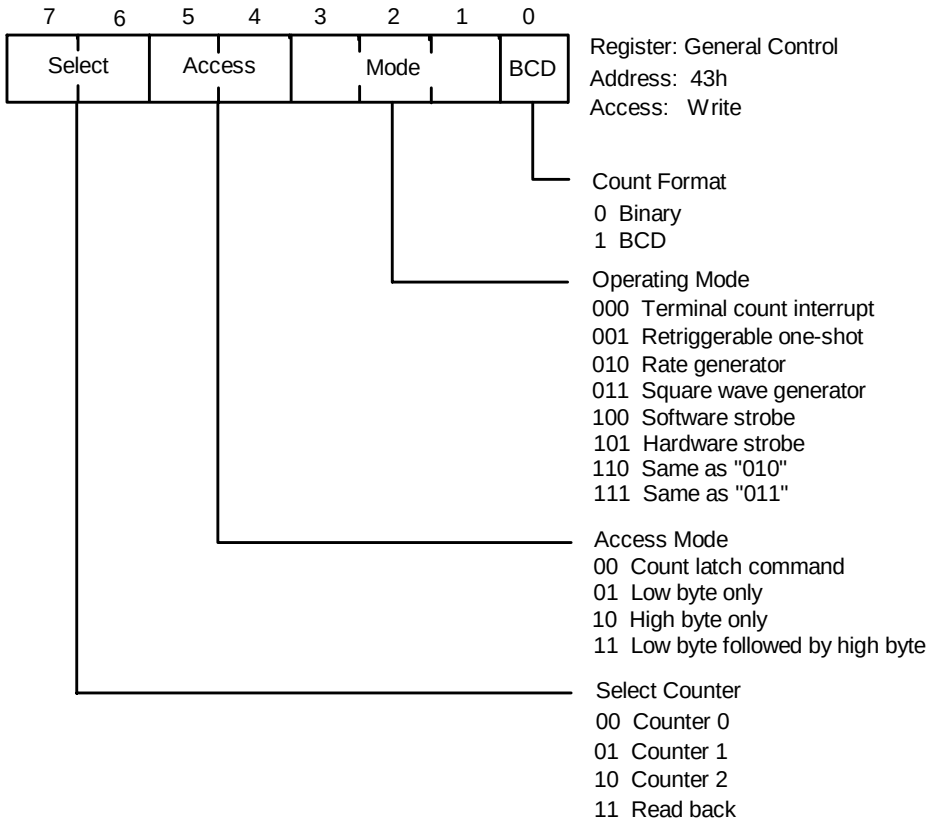
Status Register

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Control Register

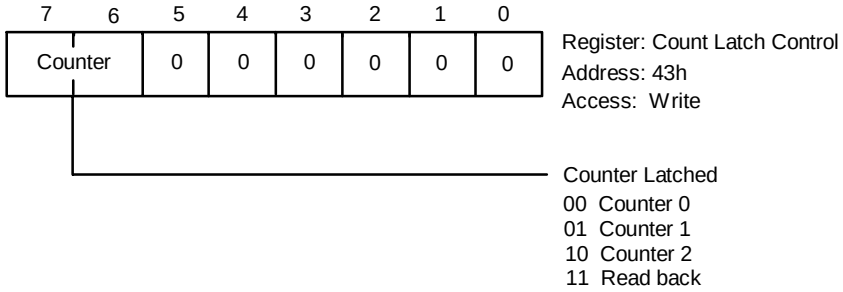
The Control register is used to initialize the counter/timers and to select the method of reading the count and status information. The Control register is best described by dividing it into three formats as illustrated in the following figures.

General Control Register



General Control Register

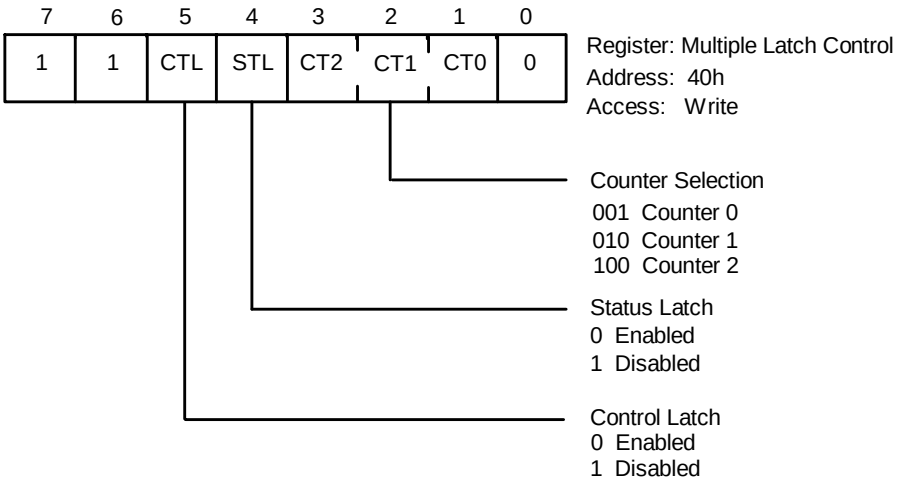
Count Latch Control Register



Count Latch Control Register

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Multiple Latch Control Register



Multiple Latch Control Register

ADDITIONAL INFORMATION

Refer to the *Ziatech Industrial Computer System Manual* for more information on the operating system's use of the counter/timers. Refer to the Intel *Peripheral Components, 1995* data book for more information on the 8254 counter/timer operating modes.

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CHAPTER 6. DMA CONTROLLER

This chapter provides an overview of ZT 8905 DMA architecture and DMA controller operation. Descriptions of DMA controller programmable registers are also included.

ZT 8905 SPECIFICS

The ZT 8905 includes two cascaded, Intel-compatible, 8237 Direct Memory Access controllers that provide a programmable interface for direct transfers between peripherals and main memory. Seven channels of DMA are supported, with up to four devices located on the STD 32 bus. The DMA controllers used on the ZT 8905 are supersets of the 8237 device, supporting 32-bit memory accesses, higher speed transfers, and the PCI protocol. Features of the DMA controllers include:

- 8237 Compatible/superset
- Seven DMA Channel support
- 32-bit memory addressing
- Compatible, TYPE A, TYPE B, TYPE F transfer rates
- Fixed or rotating priorities
- PCI Bus mastering

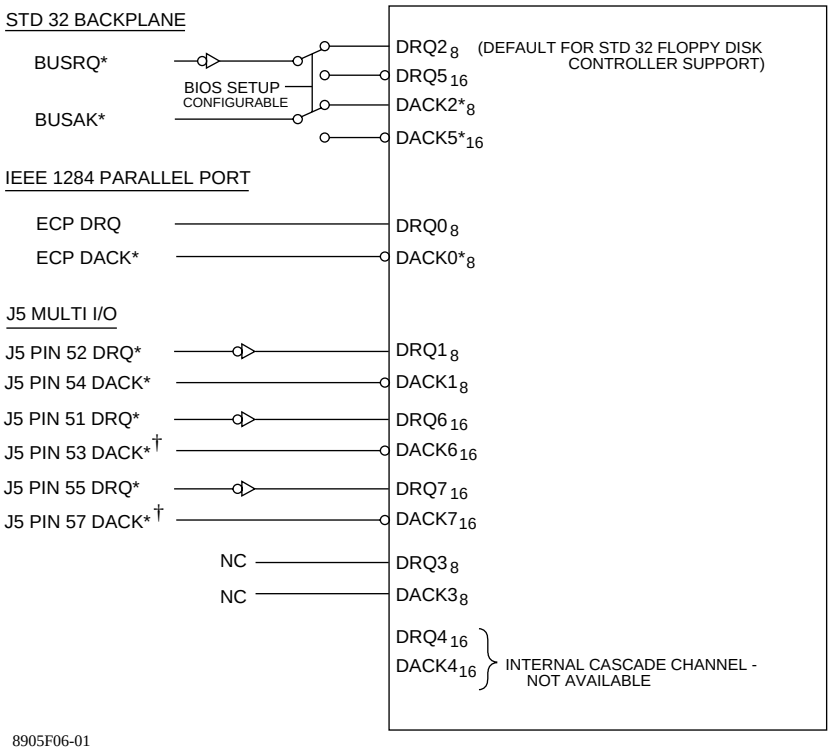
The DMA architecture is illustrated in the "DMA Architecture" figure on the following page. DMA is configured through screen 2 of the BIOS SETUP utility and allows the user to set up the DMA architecture for STD 32 support. For more on the BIOS SETUP utility, see the section "BIOS SETUP Overview" in Appendix A..

Backplane: DMA service is available for the BUSRQ*/BUSAK signals on the STD 32 backplane. Normally, these signals are used for backplane floppy disk controller servicing via DMA channel 2. If a floppy disk controller is not used in the system, SETUP alternately allows BUSRQ*/BUSAK* to be serviced by DMA Channel 5 for 16-bit peripherals. If the floppy disk controller is enabled in SETUP, only DMA Channel 2 is allowed for BUSRQ*/BUSAK*.

Frontplane: Three channels of DMA are supported via the Multi-I/O connector (J5). Channels 1, 6, and 7 can be used by STD 32 peripherals for DMA servicing.

Local: The on-board IEEE 1234 Parallel Port can be configured to use DMA channel 0 for data transfers. The Parallel Port must be configured for ECP mode to use DMA.

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† Not connected by default. Consult Cuttable Trace CT1, CT2 (Frontplane DMA) in Appendix A for details.

DMA Architecture

PROGRAMMABLE REGISTERS

Each DMA controller is managed through the 16 I/O port addresses shown in the "Slave DMA I/O Port Addressing" table. Page registers extend the 16-bit DMA address to the full 24-bit address space available on the ZT 8905. I/O port addressing for the DMA page registers is given in the "DMA Page I/O Port Addressing" and "DMA Extended Page (A24-31) I/O Port Addressing" tables. These tables are shown on the following page.

The topics that follow illustrate the DMA controller programmable registers.

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Slave DMA I/O Port Addressing

Address Slave	Address Master	Register	Operation
0	C0	Channel 0 Base/Current Address	Write
		Channel 0 Current Address	Read
1	C2	Channel 0 Base/Current Count	Write
		Channel 0 Current Count	Read
2	C4	Channel 1 Base/Current Address	Write
		Channel 1 Current Address	Read
3	C6	Channel 1 Base/Current Count	Write
		Channel 1 Current Count	Read
4	C8	Channel 2 Base/Current Address	Write
		Channel 2 Current Address	Read
5	CA	Channel 2 Base/Current Count	Write
		Channel 2 Current Count	Read
6	CC	Channel 3 Base/Current Address	Write
		Channel 3 Current Address	Read
7	CE	Channel 3 Base/Current Count	Write
		Channel 3 Current Count	Read
8	D0	Status	Read
		Command	Write
9	D2	Write Request	Write
A	D4	Write Single Mask	Write
B	D6	Write Mode	Write
C	D8	Clear Byte Pointer	Write
D	DA	Clear Master	Write
E	DC	Clear Mask	Write
F	DE	Write Mask	Write

DMA Page I/O Port Addressing

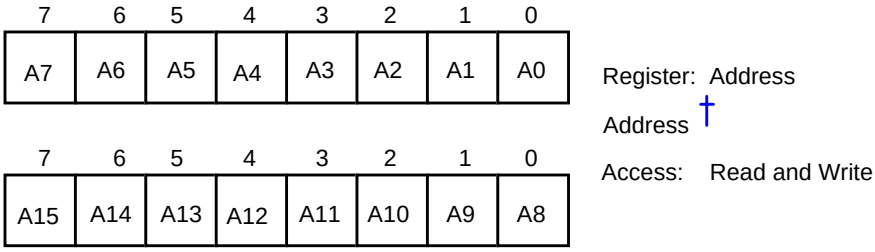
Address	Register	Operation
87h	Channel 0 A16-23 Address	Read/Write
83h	Channel 1 A16-23 Address	Read/Write
81h	Channel 2 A16-23 Address	Read/Write
81h	Channel 2 A16-23 Address	Read/Write
82h	Channel 3 A16-23 Address	Read/Write
8Bh	Channel 5 A16-23 Address	Read/Write
89h	Channel 6 A16-23 Address	Read/Write
8Ah	Channel 7 A16-23 Address	Read/Write

DMA Extended Page (A24-31) I/O Port Addressing

Address	Register	Operation
487h	Channel 0 A24-31 Address	Read/Write
483h	Channel 1 A24-31 Address	Read/Write
481h	Channel 2 A24-31 Address	Read/Write
481h	Channel 3 A24-31 Address	Read/Write
48Bh	Channel 5 A24-31 Address	Read/Write
489h	Channel 6 A24-31 Address	Read/Write
48Ah	Channel 7 A24-31 Address	Read/Write

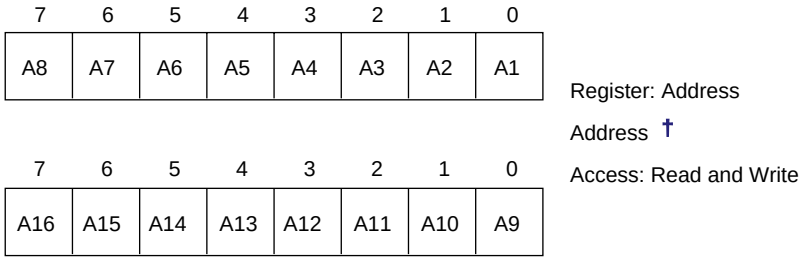
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Address Register



Address Register (8-bit I/O)

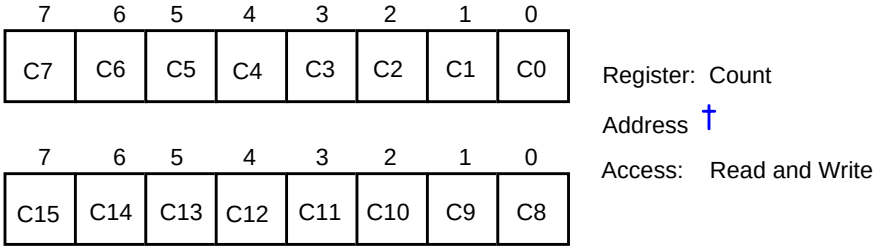
When programming a DMA channel configured for 16-bit I/O, the address is shifted as shown below.



Address Register (16-bit I/O)

† See the "Slave DMA I/O Port Addressing" table on the previous page.

Count Register

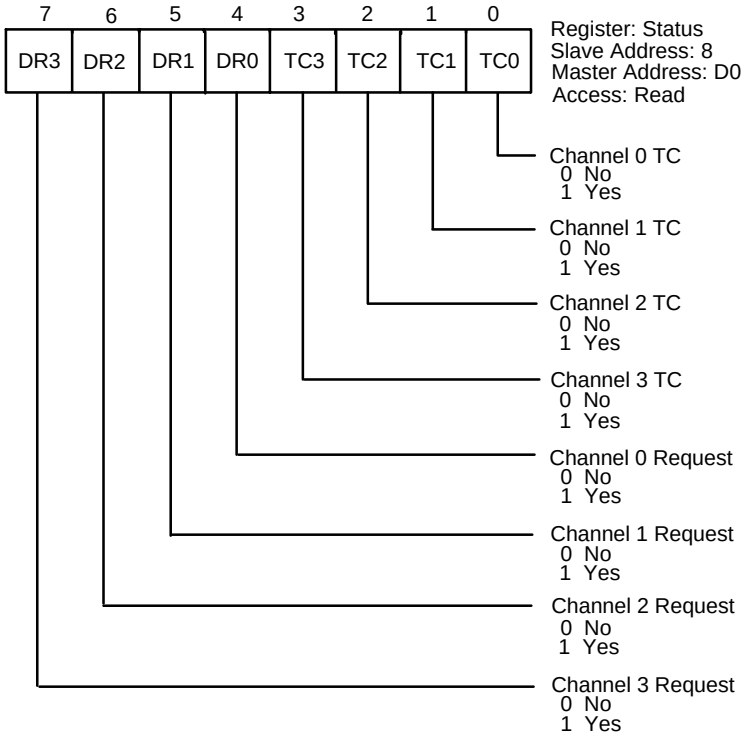


Count Register

† See the "Slave DMA I/O Port Addressing" table on the previous page.

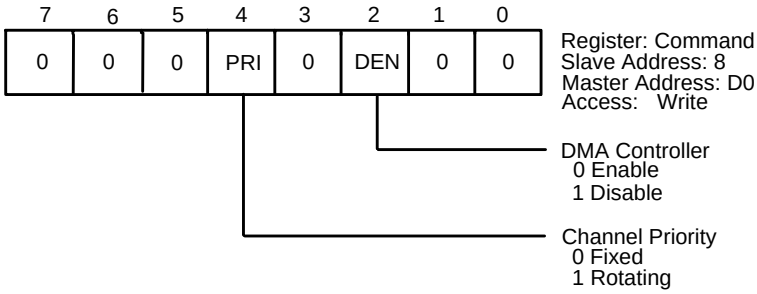
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Status Register



Status Register

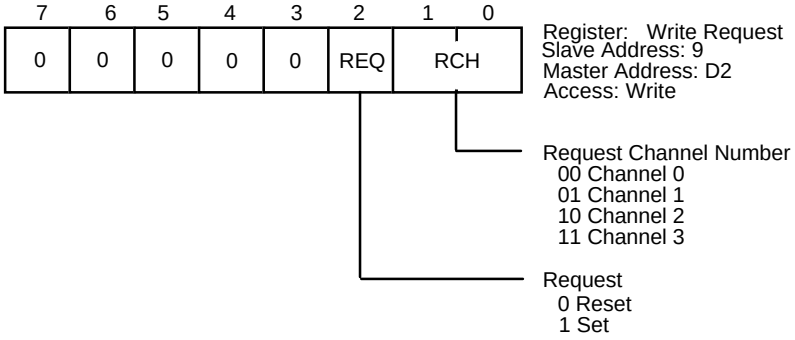
Command Register



Command Register

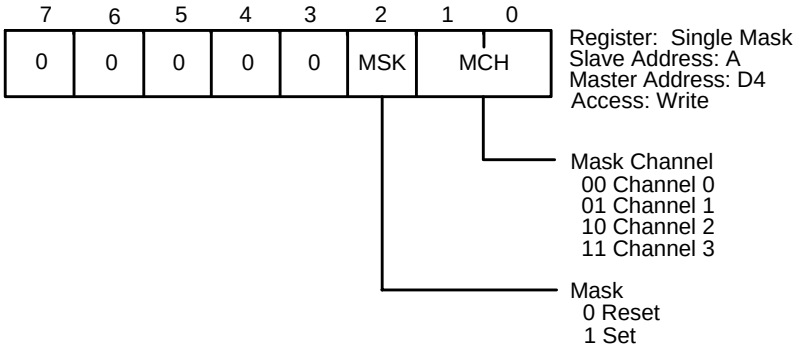
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Write Request Register



Write Request Register

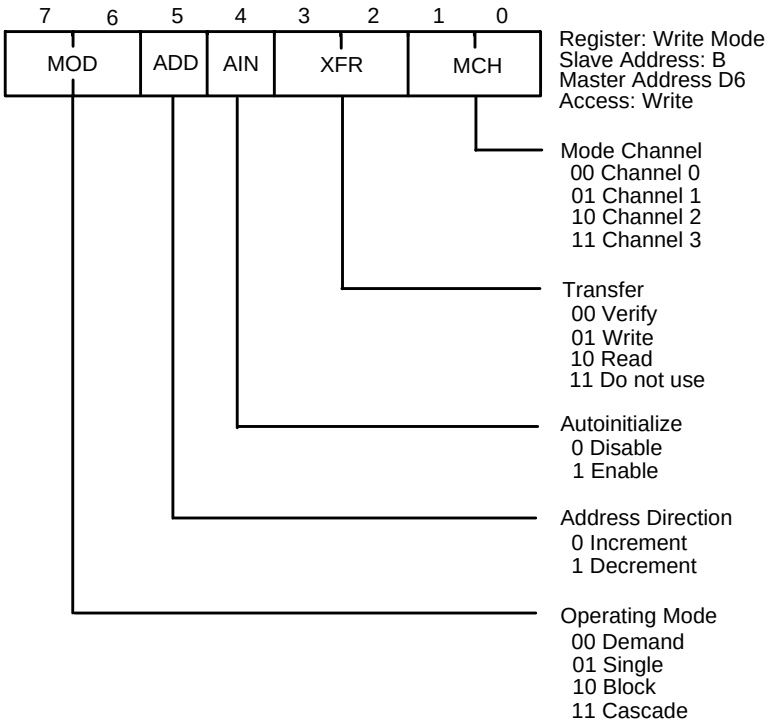
Write Single Mask Register



Write Single Mask Register

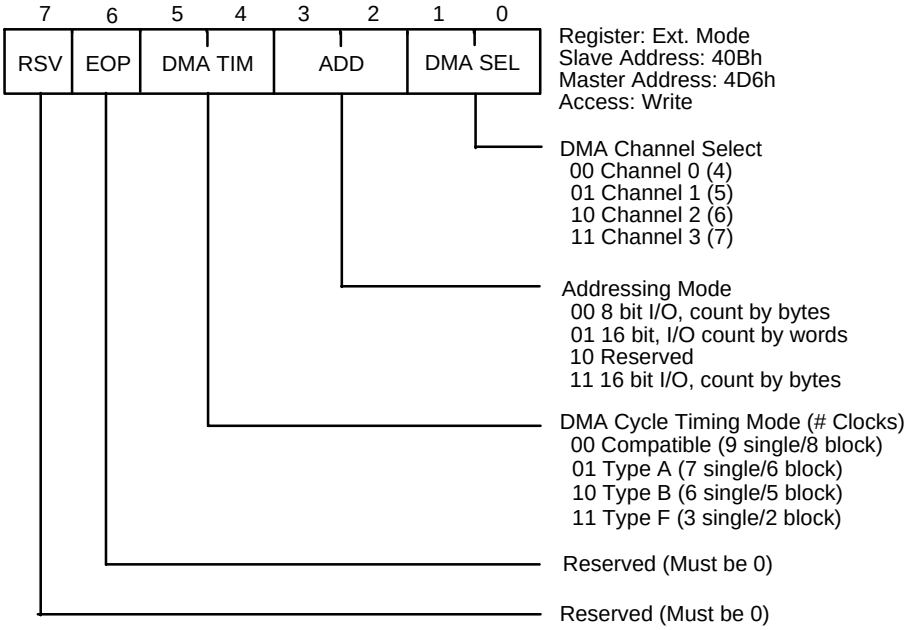
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Write Mode Register



Write Mode Register

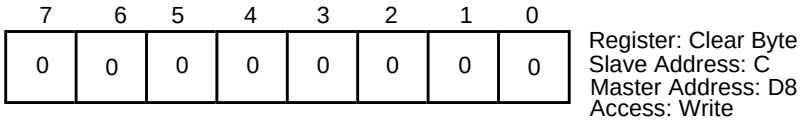
DMA Extended Mode Register



DMA Extended Mode Register

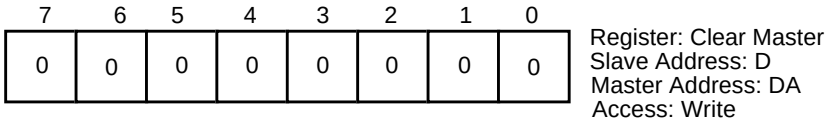
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Clear Byte Register



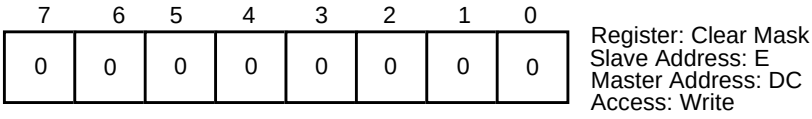
Clear Byte Register

Clear Master Register



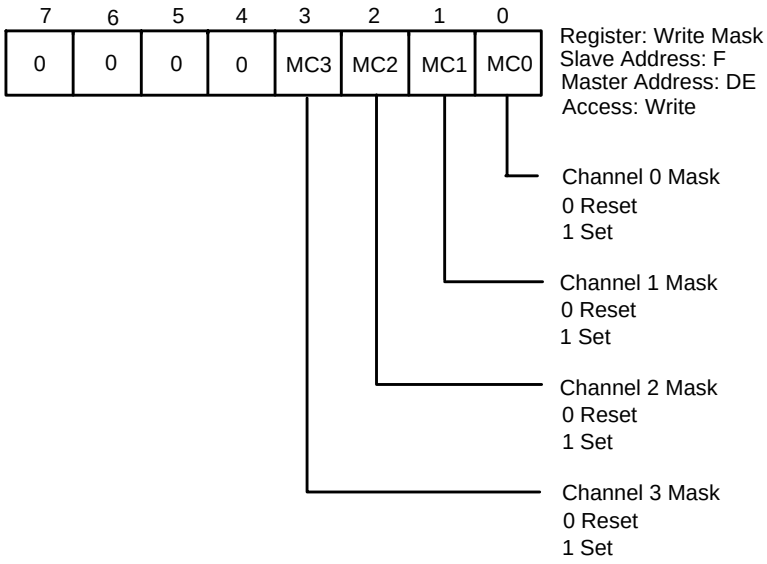
Clear Master Register

Clear Mask Register



Clear Mask Register

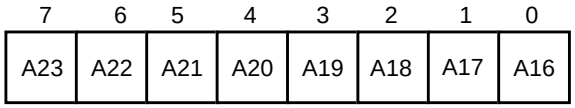
Write Mask Register



Write Mask Register

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DMA Page Register

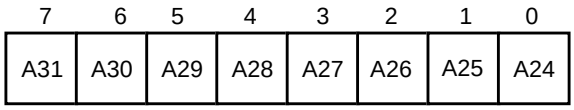


Register: DMA Page
Address †
Access: Read and Write

DMA Page Register

† See the "DMA Page I/O Port Addressing" table earlier in this chapter.

DMA Extended Page Register



Register: DMA Extended Page
Address †
Access: Read and Write

DMA Extended Page Register

† See the "DMA Extended Page (A24-31) I/O Port Addressing" table earlier in this chapter.

ADDITIONAL INFORMATION

- For more information on the operating system's use of the interrupt inputs, refer to the *Ziatech Industrial Computer System Manual*.
- For more information on the 8237 DMA controller operating modes, refer to the Intel™ *Peripherals Components, 1995* data book.
- Information on the DMA Controller may be found in the ALI® *Preliminary Data Sheet, Sept. 1994* for the Aladdin™ chipset (part #1449).

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CHAPTER 7. REAL-TIME CLOCK

The ZT 8905 includes one Motorola-compatible 146818 real-time clock. The real-time clock provides clock and 100-year calendar information in addition to 242 bytes of CMOS setup static RAM. These functions are battery backed for continuous operation even in the absence of system power. The RAM is used by the operating system BIOS to store configuration information. The major features of the real-time clock are listed below.

- Timekeeping to a 1 second resolution
- 50 bytes of CMOS setup RAM
- Leap year compensation
- Daylight Savings Time compensation
- Periodic, Alarm, and Update Ended interrupts
- Battery backed

PROGRAMMABLE REGISTERS

The real-time clock includes 64 register locations. These registers are accessed through I/O port locations 70h and 71h. A real-time clock register is accessed by first writing the offset address of the register to I/O port location 70h. Data is then transferred to or from the register through I/O port location 71h. This sequence must be repeated to read the same register a second time. The I/O port addressing for the real-time clock is given in the "Real-Time Clock Register Addressing" table below.

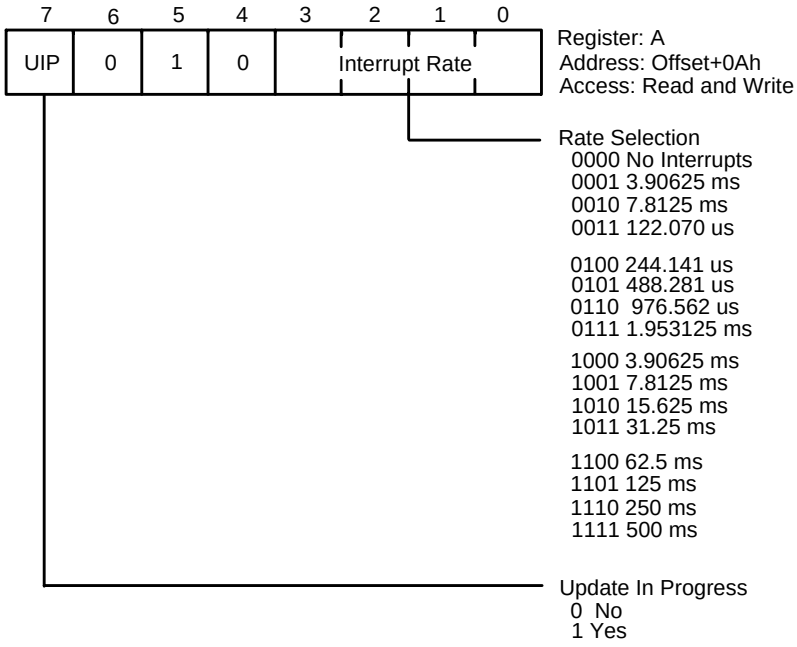
The topics that follow illustrate the programmable registers for the real-time clock.

Real-Time Clock Register Addressing

Address Offset	Function	Range
0h	Time-Seconds	0-59
1h	Alarm-Seconds	0-59
2h	Time-Minutes	0-59
3h	Alarm-Minutes	0-59
4h	Time-Hours (12 hour mode)	1-12
4h	Time-Hours (24 hour mode)	0-23
5h	Alarm-Hours	0-23
6h	Day of Week	1-7
7h	Date of Month	1-31
8h	Month	1-12
9h	Year	0-99
Ah-Dh	Register A-D	----
Eh-3Fh	General Purpose	----

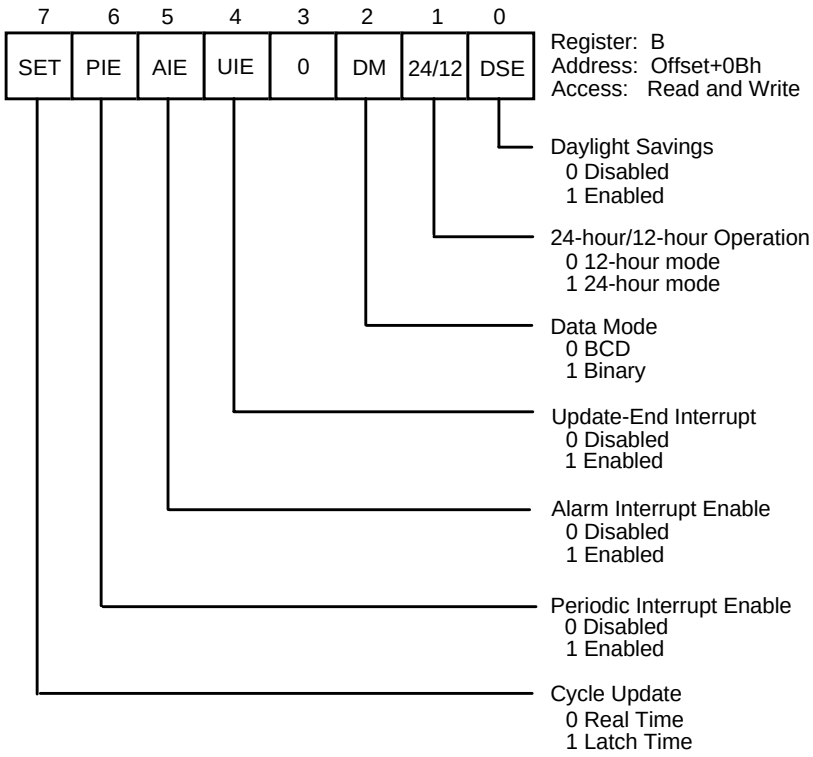
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Register A



Register A

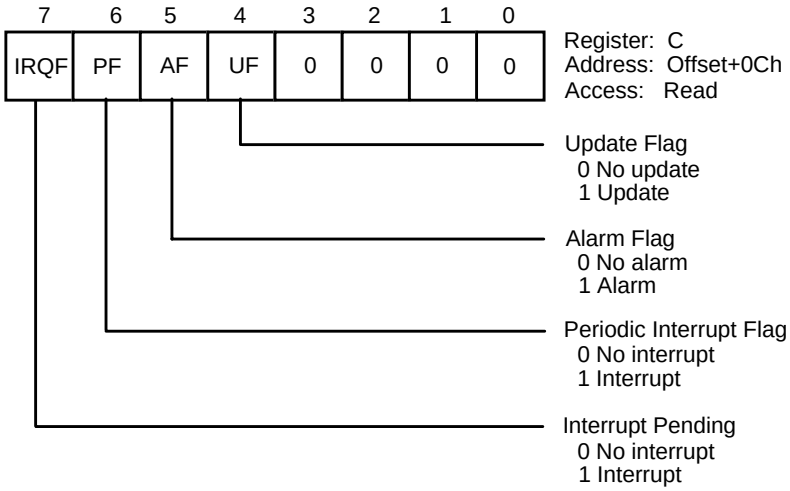
Register B



Register B

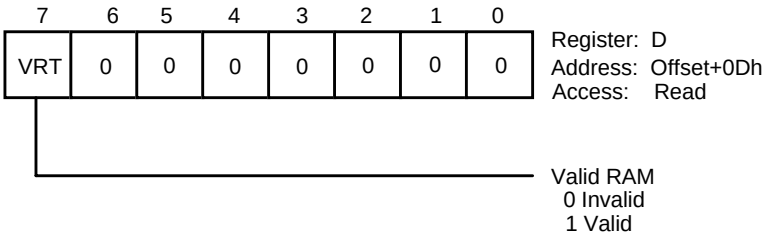
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Register C



Register C

Register D



Register D

ADDITIONAL INFORMATION

Refer to the National Semiconductor PC87303 data book for more information on the real-time clock operating modes.

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CHAPTER 8. SERIAL CONTROLLER

This chapter discusses operation of the two ZT 8905 serial ports. Each channel is compatible with the industry standard 16550 serial port, including support for a 16 byte FIFO for read and write operations.

ZT 8905 SPECIFICS

The ZT 8905 includes two serial ports that are compatible with the industry standard 16550. The drivers for each serial port are implemented with 5 V charge pump technology to eliminate the need for a ±12 V supply. The serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115.2 Kbaud. Both channels are supplied as DTE configured devices through the multi-I/O connector, J5. The ZT 90205 cable assembly allows each channel to be interfaced directly to 9-pin D-Shell serial devices, as used in PC applications. Each port may be disabled to allow for STD 32 based COM ports (for example, an off-board modem) to be used.

The major features of each serial port are listed below.

- Two RS-232 channels
- 16550 compatible
- Drivers do not require ±12 V
- Baud rates up to 115.2 Kbaud
- Polled and interrupt operation
- Loopback diagnostics

Details for the two serial ports on the ZT 8905 are discussed in the following topics.

Address Mapping

The address mapping for the PC standard architecture and the ZT 8905 is shown below.

Serial Channel	PC Port Address	ZT 8905 Port Address
COM1	3F8-3FF	3F8-3FF or disabled for off-board COM support
COM2	2F8-2FF	2F8-2FF or disabled for off-board COM support

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Interrupt Selection

The interrupt mapping for the PC standard architecture and the ZT 8905 is shown below. Different interrupt levels for COM1 and COM2 interrupts are selectable through screen 2 of the BIOS SETUP utility. For more on the BIOS SETUP utility, see the section "BIOS SETUP Overview" in Appendix A.

Serial Channel	PC Interrupt	ZT 8905 Interrupt
COM1	IR4	IR4 or disabled for off-board COM support
COM2	IR3	IR3 or disabled for off-board COM support

Handshake Signals

The PC architecture includes Transmit Data (TXD), Receive Data (RXD), Request To Send (RTS), Clear To Send (CTS), Data Set Ready (DSR), Data Terminal Ready (DTR), Ring Indicator (RI), and Data Carrier Detect (DCD).

Serial Channel Interface

The serial ports are configured as DTE and are available through the 100-pin Multi-I/O connector (J5) The optional ZT 90205 cable converts the serial port interface to standard 9-pin D-shell connectors. The J5 connector pin assignments are accessible through the "J5 Multi-I/O Connector" topic in Appendix B.

PROGRAMMABLE REGISTERS

There are six registers for initializing and controlling each serial channel. The "Serial Controller Register Addressing" table below shows the I/O port addressing for the COM port registers. The topics that follow illustrate the 16-bit divisor latch, baud rate divisors, and the six programmable registers for each serial channel.

Serial Controller Register Addressing

COM 1 Address	COM 2 Address	Register	Operation
03F8h (DIV=0)	02F8h (DIV=0)	Receive Buffer	Read
03F8h (DIV=0)	02F8h (DIV=0)	Transmit Buffer	Write
03F8h (DIV=1)	02F8h (DIV=1)	Divisor Latch LSB	Read/Write
03F9h (DIV=0)	02F9h (DIV=0)	Interrupt Control	Read/Write
03F9h (DIV=1)	02F9h (DIV=1)	Divisor Latch MSB	Read/Write
03FAh	02FAh	Interrupt Status	Read
03FBh	02FBh	Line Control	Read/Write
03FCh	02FCh	Modem Control	Read/Write
03FDh	02FDh	Line Status	Read
03FEh	02FEh	Modem Status	Read
03FFh	02FFh	Reserved	

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Baud Rate Divisors

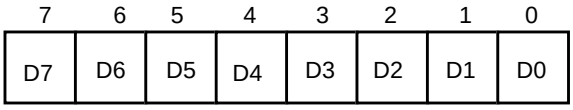
The "Divisor Latch LSB" and "Divisor Latch MSB" figures that follow illustrate the 16-bit divisor latch. The "Baud Rate Divisors" table below lists the divisors for popular baud rates. It also includes the percent error based on the difference between the exact divisor for a specified baud rate and the divisor obtainable with a 16-bit integer format. To guarantee proper operation, the percentage error should never be greater than four.

Baud Rate Divisors Table

Baud Rate	Divisor (dec/hex)	Percent Error
50	2304/1440h	0
75	1536/960h	0
150	768/480h	0
300	384/240h	0
600	192/120h	0
1200	96/60h	0
1800	64/40h	0
2000	58/3Ah	0.69
2400	48/30h	0
3600	32/20h	0
4800	24/18h	0
7200	16/10h	0
9600	12/Ch	0
19200	6/6h	0
38400	3/3h	0
56000	2/2h	2.86
57600	2/2h	0
115200	1/1h	0

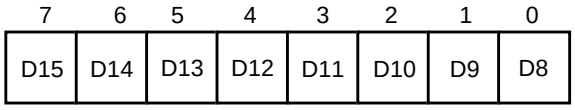
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Divisor Latch LSB and MSB



Register: Divisor Latch LSB
Address: 2F8/3F8h DIV=1
Access: Read and Write

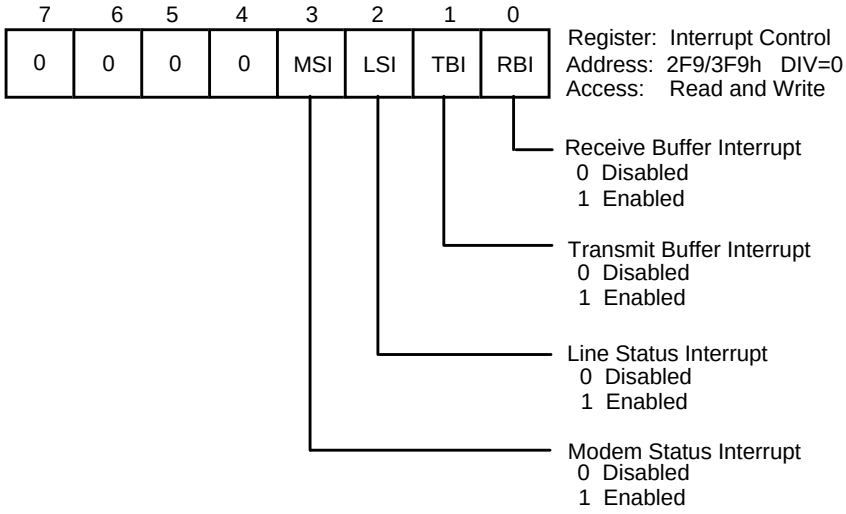
Divisor Latch LSB



Register: Divisor Latch MSB
Address: 2F9/3F9h DIV=1
Access: Read and Write

Divisor Latch MSB

Interrupt Control Register



Register: Interrupt Control
Address: 2F9/3F9h DIV=0
Access: Read and Write

Receive Buffer Interrupt
0 Disabled
1 Enabled

Transmit Buffer Interrupt
0 Disabled
1 Enabled

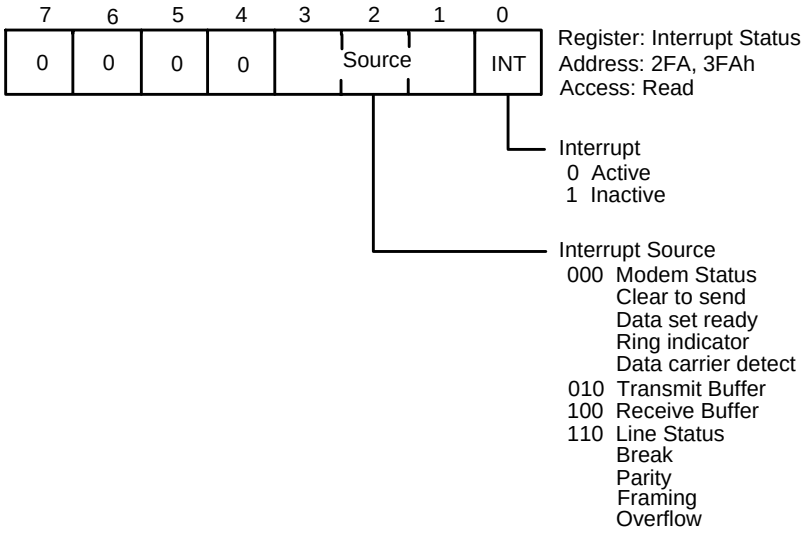
Line Status Interrupt
0 Disabled
1 Enabled

Modem Status Interrupt
0 Disabled
1 Enabled

Interrupt Control Register

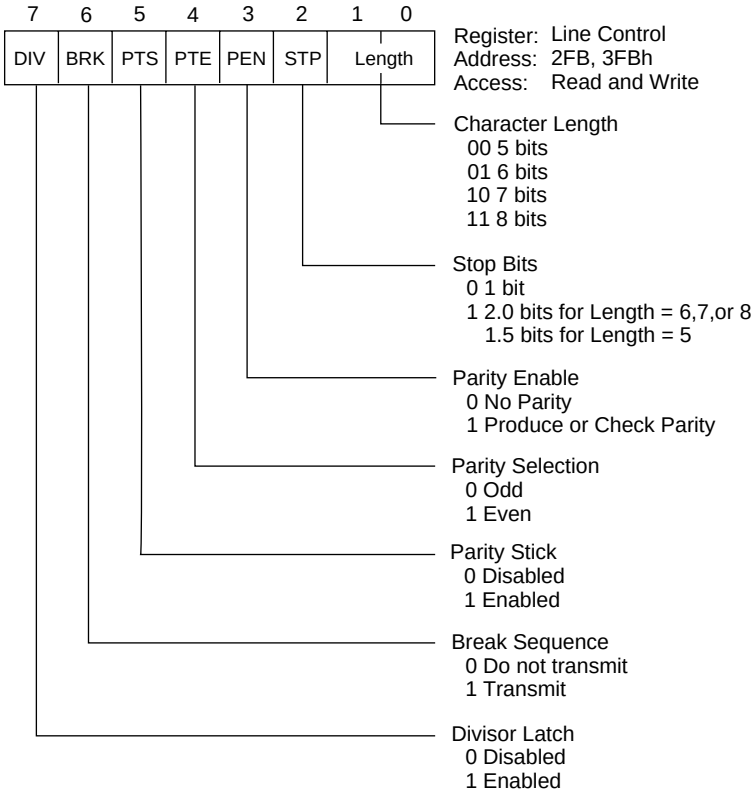
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Interrupt Status Register



Interrupt Status Register

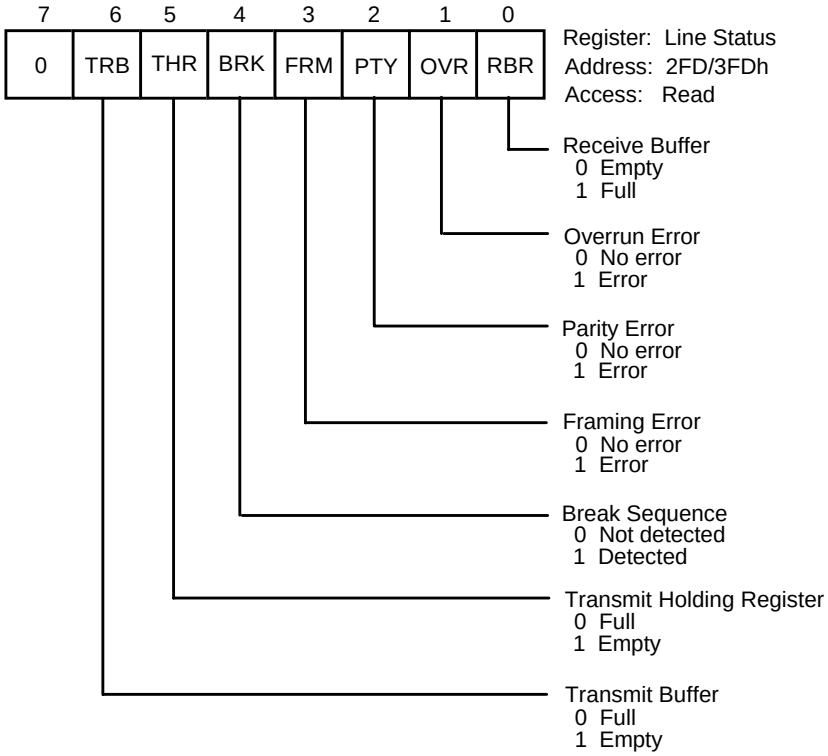
Line Control Register



Line Control Register

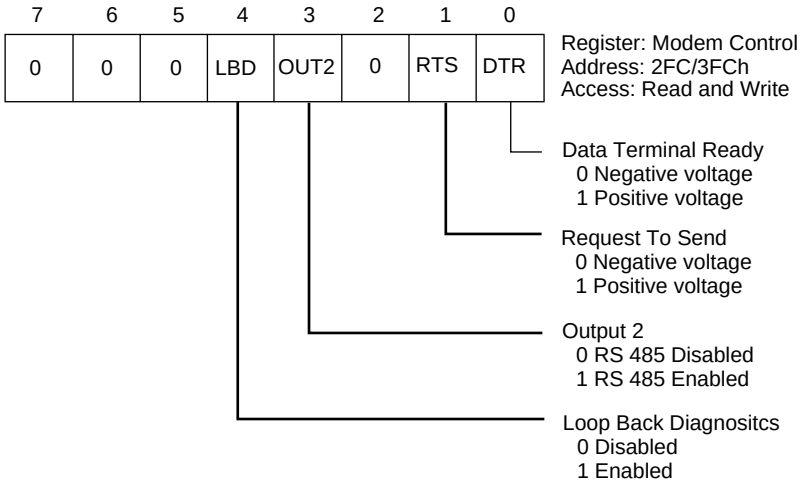
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Line Status Register



Line Status Register

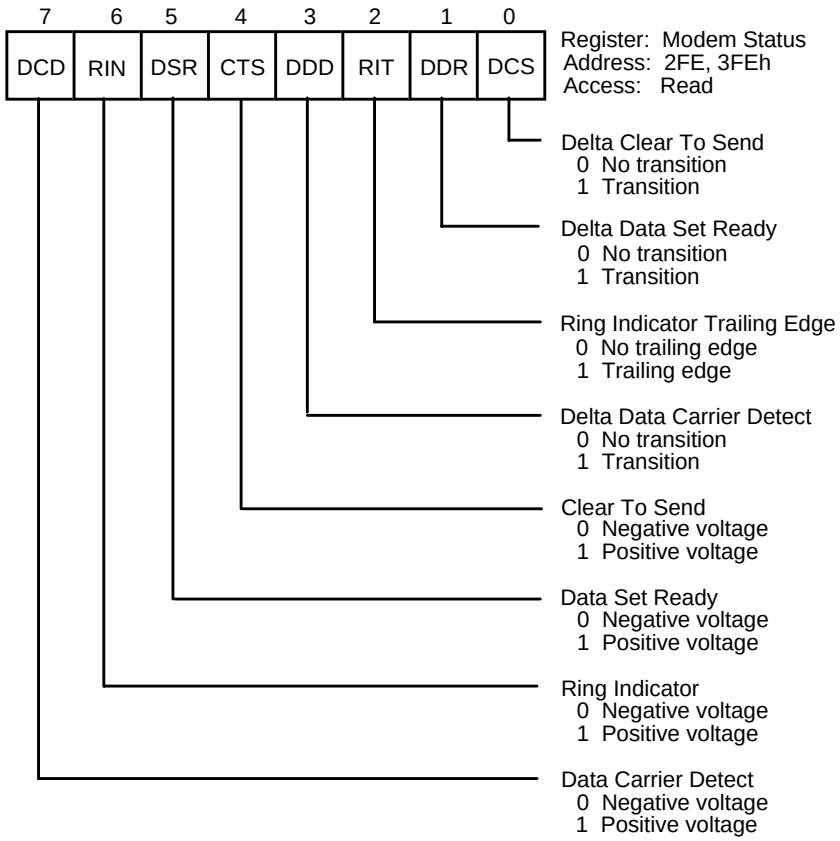
Modem Control Register



Modem Control Register

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Modem Status Register



Modem Status Register

ADDITIONAL INFORMATION

Refer to the National Semiconductor PC87C303 data book for more information on the serial controller operating modes.

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CHAPTER 9. IEEE-1284 PARALLEL PORT INTERFACE

The ZT 8905 supports an IEEE-1284 compatible printer port interface, available through the Multi-I/O connector (J5).

The printer port can be configured in Normal (compatibility), Extended, EPP, or ECP modes through screen 1 of the BIOS SETUP utility (discussed in the section "BIOS SETUP Overview" in Appendix A).

The ZT 90206 cable assembly allows the on-board LPT1 channel to interface directly to 25-pin D-Shell parallel port devices, as used in PC applications. The on-board port may be disabled to allow use of STD 32 based parallel interfaces.

PARALLEL PORT CONFIGURATION OPTIONS

The different modes for the printer port are described below. Details for the parallel port on the ZT 8905 are discussed in the following topics.

Parallel Port Mode	Description	Max. Data Rate
Normal (compatibility) (Default)	Uni-directional data configuration. The original PC-AT Mode. Also known as "nibble mode" because the four status bits in the cable are used for feedback from devices such as tape back-up units (when restoring data from a tape). Software based protocol.	50-150 kbps
Extended	Bi-directional data transfer capability. Similar to Normal mode, but allows 8-bit data in both directions. Faster for interfaces needing to supply data to the computer (e.g., scanners, tape back-up). Software based protocol.	50-150 kbps
EPP	Enhanced Parallel Port. Hardware based handshaking of the data transfers provide single I/O instruction data transfers in read and write operations. Register superset of Normal/Extended modes.	500 Kbps-2 Mbps
ECP	IEEE-1284 Extended Capability Port. Similar to EPP, but register set is strictly defined. Adds FIFO's for read/write operations. ECP devices require IEEE-1284 compliant cabling and buffers. The ZT 8905 supplies compliant buffers - cabling is available from other sources.	500 Kbps-2 Mbps

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ADDRESS MAPPING

The address mapping for the PC standard architecture and the ZT 8905 is shown below. The on-board port may be disabled to allow an STD 32 LPT port to be used.

Parallel Port	PC Port Address	ZT 8905 Port Address
LPT1	3BC (typically)	378-37F - Normal, Extended, EPP Modes
		378-37A, 778-77A - ECP Mode

INTERRUPT SELECTION

The interrupt mapping for the PC standard architecture and the ZT 8905 is shown below.

Parallel Port	PC Interrupt	ZT 8905 Interrupt
LPT1	IR5	IR7 or disabled for off-board LPT support

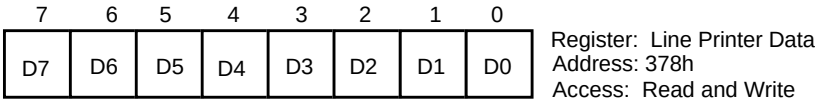
DMA SELECTION

DMA may be configured for ECP mode in software. DMA channel 0 is dedicated for ECP support and may be used by application software. The BIOS does not use DMA for any data transfers. Applications needing DMA support must configure the parallel port with appropriate initialization code.

PROGRAMMABLE REGISTERS

The following topics illustrate the programmable registers for the Normal/Extended mode parallel port interface. For EPP and ECP information, consult the National Semiconductor PC87303 data sheet (National LIT# 112904-001)

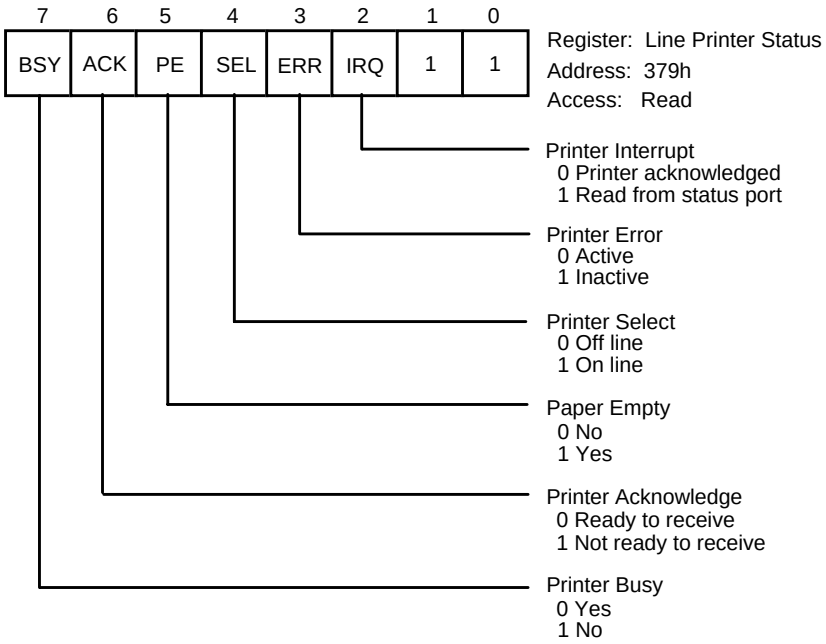
Line Printer Data Register



Line Printer Data Register

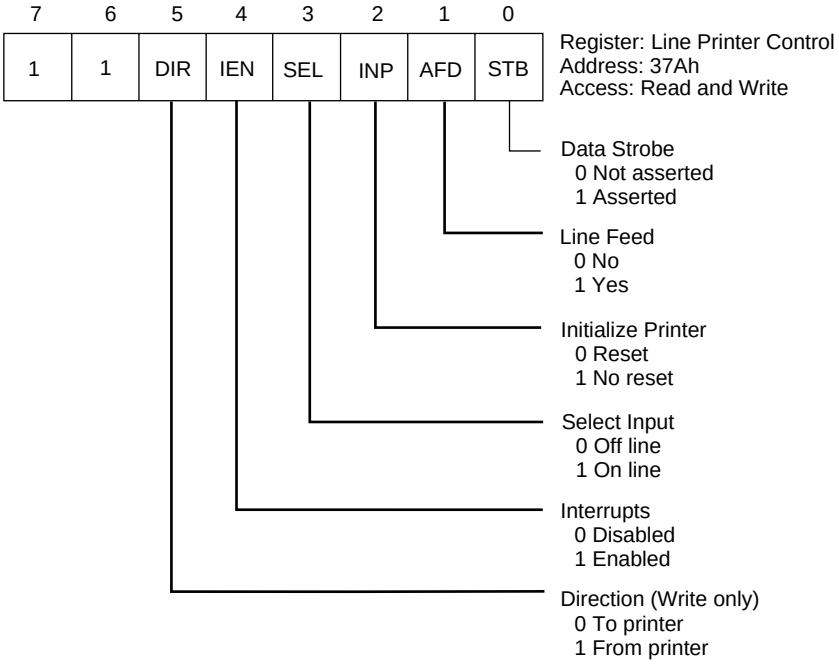
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Line Printer Status Register



Line Printer Status Register

Line Printer Control Register



Line Printer Control Register

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ADDITIONAL INFORMATION

Refer to the National Semiconductor PC87303 data book (National LIT# 112904-001) for more information on the parallel controller operating modes. An excellent tutorial of IEEE-1284 can be obtained from FarPoint Communications (805) 726-4420. The IEEE-1284 specification can be obtained from the IEEE Standards Office at (800) 678-4333, ask for document number DS02709.

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CHAPTER 10. OPTIONAL IDE INTERFACE

The ZT 8905 can be purchased with a local Intelligent Drive Electronics (IDE) Hard Disk Interface attached to the bottom side of the board via a carrier board. This feature is useful for single board applications as well as STAR SYSTEMs where the ZT 8905 needs to have a local (non-shared) hard disk.

The specific size of the drive (in Megabytes) that is sold with this option may change because the hard disk drive market continually improves capacity. In general, Ziatech offers a higher capacity drive for the same or similar price when a new drive is qualified.

The on-board IDE interface is a factory load option at Ziatech. Option D1 to the ZT 8905 includes a hard disk, mounting board, and connector. When configured for local IDE operation, the ZT 8905 requires one additional slot in the STD 32 card cage. The on-board IDE hard disk is an ISA-based interface, not a PCI-based interface. The performance of the IDE interface is equivalent to an STD 32 based hard disk controller (ZT 8952 or ZT 8953), so there is no advantage to using the on-board interface other than for single board applications or STAR SYSTEMs as mentioned above.

It is not possible to configure the ZT 8905 for both on-board IDE operation and STD 32 IDE operation.

The ZT 8905 provides a green hard disk activity light for local IDE accesses.

HARD DISK MOUNTING

A carrier board is provided for the IDE hard disk. This carrier board has a special connector that interfaces to connector J7 on the ZT 8905 to provide the IDE signals to the drive. No cables are used for the interconnection. The carrier board is mounted on standoffs such that the board slides into an STD 32 connector, providing additional support as well as power for the hard drive unit. The integrated drive is a 2.5 inch family drive, using a 2 mm connector interface. 3.5 inch drives are not supported by the carrier board.

ENABLING THE ON-BOARD IDE CONTROLLER

In screen 1 of the BIOS SETUP utility (discussed in the section "System Configuration Overview" in Chapter 2), select "Onboard" for the IDE interface. This selection automatically configures the ZT 8905 for I/O addressing as well as interrupt support for the IDE drive mounted on the carrier board.

SINGLE BOARD APPLICATIONS

The ZT 8905 can be used in single board applications with a local IDE hard disk. The carrier board provides mounting locations for such applications. Ziatech suggests that the application provide power both to the ZT 8905 STD 32 connector and the carrier board STD 32 connector. Ziatech also suggests that the carrier board and ZT 8905 connectors be physically used as a support for the assembly.

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STAR SYSTEM APPLICATIONS

Certain STAR SYSTEM applications require that a CPU board have exclusive access to an IDE drive. This can be because the CPU is booting a unique operating system or requires isolated (non-shareable) hard disk capability for performance reasons. The on-board IDE interface addresses all of these needs, although performance is equivalent to the ZT 8952 or ZT 8953. System performance, however, is improved because the local IDE accesses do not impact the STD 32 bus, allowing other processors lower latency to system wide resources. The local processor also does not have to arbitrate for the STD 32 bus for local IDE transfers, improving its performance.

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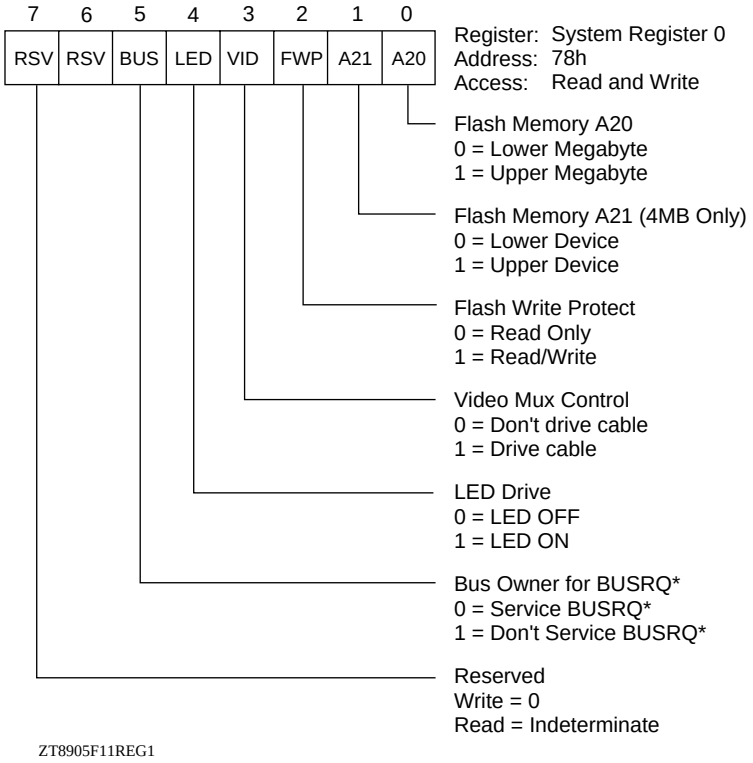
CHAPTER 11. SYSTEM REGISTERS

There are two system registers used to control and monitor a variety of functions on the ZT 8905. Each register is read/write capable. Normally, only the system BIOS will use the registers, but they are documented for application use as needed. Care must be taken when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under its control.

PROGRAMMABLE REGISTERS

The following topics illustrate the two System registers.

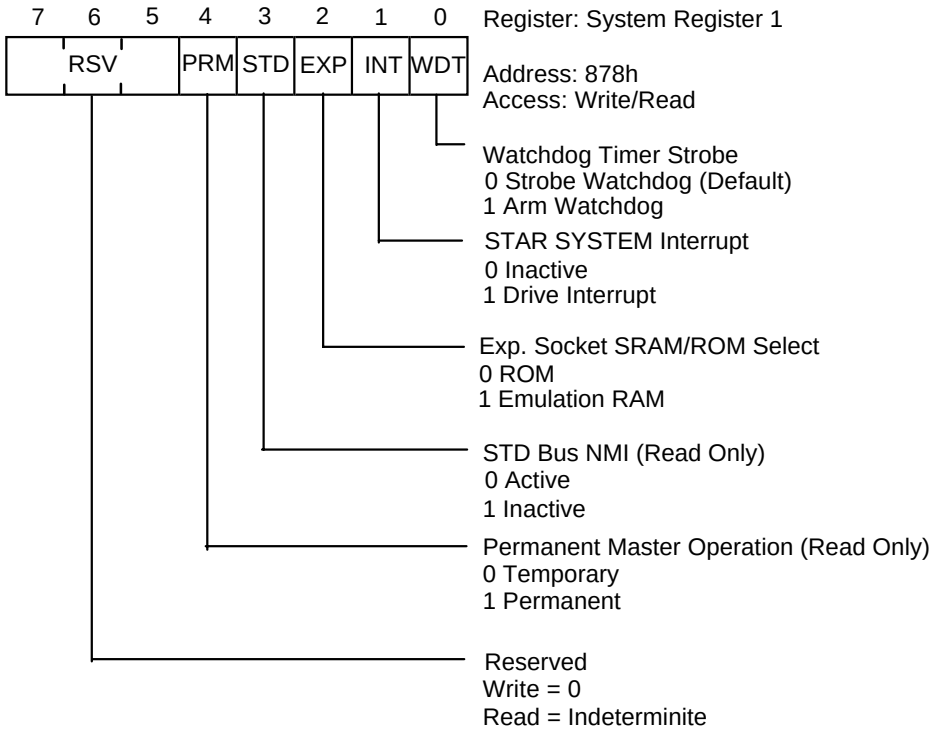
System Register 0



System Register 0

System Register 0

System Register 1



System Register 1

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CHAPTER 12. WATCHDOG TIMER

The primary function of the watchdog timer is to monitor ZT 8905 operation and take corrective action if the system fails to function as programmed. The major features of the watchdog timer are listed below.

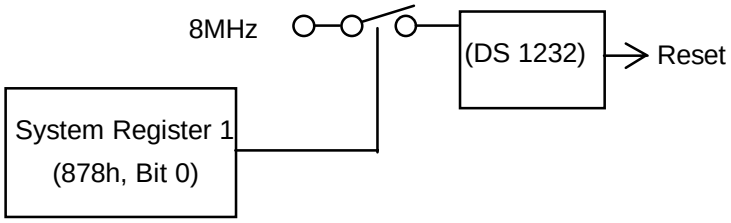
- Single-stage
- Enabled and disabled through software control
- Armed and strobed through software control

WATCHDOG TIMER OPERATION

The watchdog timer architecture is illustrated in the "Watchdog Timer Architecture" figure below. The watchdog timer is implemented in the Dallas Semiconductor DS1232 system monitor.

After power on or reset, the watchdog function is disabled, meaning that the watchdog is continually being strobed by an 8 MHz signal. Bit 0 of System Register 1 (878h) must be programmed with a logical one to enable the watchdog timer to begin operation. If the watchdog is allowed to expire, a reset is generated. If the ZT 8905 is configured as a permanent master, the reset extends to the STD bus. If the ZT 8905 is configured as a temporary master, the reset remains local. To strobe the watchdog, Bit 0 of System Register 1 (878h) must be written with a logical 0 and then a logical 1.

The watchdog timeout period is fixed at 500 ms minimum and 2000 ms maximum. Software must strobe the watchdog timer within 500 ms to guarantee that the system is not reset.



WatchDog Timer Architecture

ADDITIONAL INFORMATION

Refer to the Dallas Semiconductor DS1232 data sheet for more information on the watchdog timer and the associated operating modes.

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CHAPTER 13. PCI MEZZANINE LOCAL BUS

The ZT 8905 includes a PCI compatible local bus interface to industry standard PCI mezzanine devices. The bus operates at half of the CPU *external* clock speed. Ziatech offers PCI peripheral adapters designed specifically for this local bus interface. These adapters give superior performance over STD bus solutions by running with up to four times the data width and up to four times the operating frequency. Major features of the PCI interface are listed below.

- 25, 30, or 33 MHz operation (Determined by CPU speed)
- Reduces STD bus traffic by keeping all PCI operations local
- Single-slot occupancy capable (VGA)

PCI OPERATION FREQUENCY

The PCI operating frequency is derived from the frequency at which the Pentium CPU is operating. The Pentium is available with several different internal clock multipliers (1.5X, 2X, 2.5X, and 3X).

Processor Speed (MHz)	Internal Clock Multiplier	External Processor Speed	PCI Operating Frequency
75	1.5X	50.0	25.0
90	1.5X	60.0	30.0
100	1.5X	66.6	33.3
120	2.0X	60.0	30.0
133	2.0X	66.6	33.3
150	2.5X	60.0	30.0
166	2.5X	66.6	33.3
180	3.0	60.0	30.0
200	3.0	66.6	33.3

ADDITIONAL INFORMATION

Refer to the individual peripheral data sheets for additional details and installation and operating instructions.

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CHAPTER 14. PROGRAMMABLE LED

The ZT 8905 includes two Light-Emitting Diodes (LEDs). A green LED for the optional IDE disk drive is mounted at the bottom right corner of the board when viewed from the top with the gold fingers to the left. A red general purpose LED is located just under the extractor. The red LED is software programmable through the LED bit in System register 0 (see Chapter 11, "System Registers"). Writing a logical 0 to the LED bit turns the LED off and writing a logical 1 to the LED bit turns the LED on. The LED is turned off after a power cycle or a reset.

The LED bit is in the same register as several system level functions. It is important to preserve the state of the other bits in this register when modifying the LED status. The following code demonstrates the mechanism for modifying the LED bit:

```
;  set LED ON
cli                     ; clear interrupts
in     al, 78h          ; read current state
or     al, 10h          ; set LED bit
out    78h, al          ; output new value for register
sti                     ; re-enable interrupts

;  set LED OFF
cli                     ; clear interrupts
in     al, 78h          ; read current state
and    al, 0EFh         ; clear LED bit
out    78h, al          ; output new value for register
sti                     ; re-enable interrupts
```

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APPENDIX A. BOARD CONFIGURATION

The ZT 8905 includes several options that tailor the operation of the board to requirements of specific applications. Most of the options are selected through the BIOS SETUP mechanism. Some options cannot be software controlled and are configured with jumpers or cuttable traces. Jumper options are made by installing and removing shorting receptacles. Cuttable trace options are made by installing and removing surface mount 0 Ω resistors.

This appendix covers SETUP options, jumper options, and cuttable trace options. It also provides an illustration showing the locations of jumpers and cuttable traces on the ZT 8905.

BIOS SETUP OVERVIEW

The ZT 8905 has many features that can be configured with the BIOS SETUP utility. The SETUP utility is executed during the boot sequence when the **"s"** key is typed. In DOS systems, SETUP may be executed by running the SETUP.COM program from the command line.

BIOS SETUP Screens

The BIOS SETUP utility for the ZT 8905 is organized as two screens, listed below. †

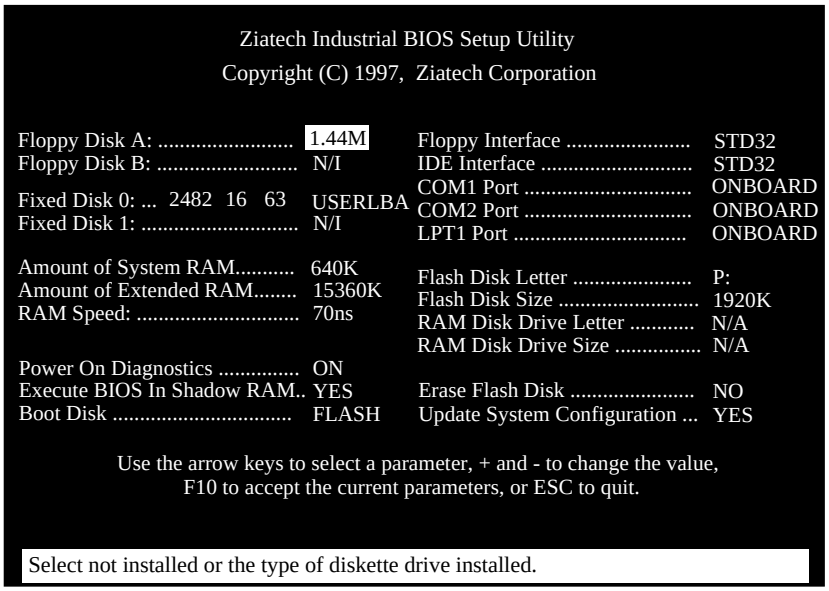
- Screen 1: **Generic option list.** Options shared among all Ziatech CPUs are listed on this screen. Base memory and extended memory size selection, boot source, hard disk type, and floppy disk type are configurable through this screen.

- Screen 2: **ZT 8905-specific SETUP options.** Options such as interrupt routing and STD 32 memory and I/O addressing are configurable through this screen. See the following topic, "ZT 8905-Specific SETUP Options," for more information.

† A third screen is used for STAR SYSTEM configuration options on permanent master CPUs. Refer to the *STD 32 STAR SYSTEM User's Manual* for more information.

The parameters in the SETUP screens are easily changed. Use the arrow keys to select a parameter, then press + or - to step through the valid choices for that parameter. A dynamic help line at the bottom of the screens helps you determine how to set each parameter. SETUP accepts only valid parameter sets: if changing one parameter invalidates another parameter, SETUP automatically updates the invalid parameter. After setting the parameters, press the F10 key to accept them. Press the Page Down and Page Up keys to switch between SETUP screens.

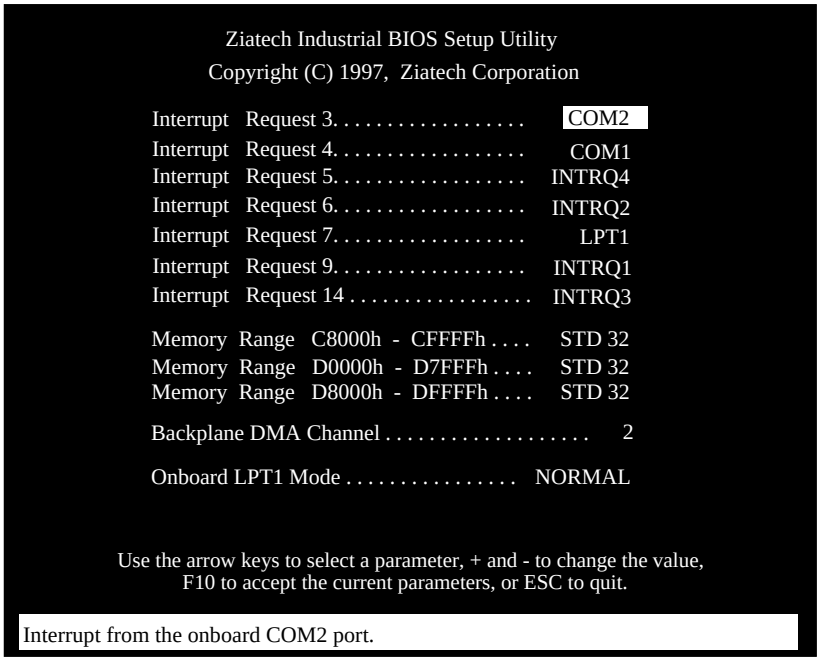
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ZT8905F02-05

BIOS SETUP Utility: Screen 1

Generic SETUP Options



ZT8905F02-06

BIOS SETUP Utility: Screen 2

ZT 8905-Specific SETUP Options

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ZT 8905-Specific SETUP Options

ZT 8905-specific SETUP options, such as interrupt routing and STD 32 memory and I/O addressing, are configurable through screen 2 of the SETUP utility and are discussed below.

- Interrupt routing

  The source for individual interrupt controller inputs is selectable through screen 2 of the SETUP utility. The STD 32 backplane interrupts, frontplane interrupts, and PCI interrupts are options.

- Backplane DMA (via BUSRQ*/BUSAK*) channel selection

  Normally, the BUSRQ*/BUSAK* signals are used to allow DMA to a backplane based floppy disk controller (for example, ZT 8954), but other devices may use this mechanism in absence of a floppy disk controller. The channel is selectable between channel 2 (for floppy disks) and channel 5 (for 16-bit operations).

- STD 32 memory address decoding

  Locations in the lower 1 Mbyte and in extended memory can be dedicated to the STD 32 bus. Regions that are configured for STD 32 cannot be used for PCI peripherals. The following regions are selectable:

  000C8000h - 000CFFFFh† (**Note:** This region is required for STAR SYSTEM operation)
  000D0000h - 000D7FFFh†
  000D8000h - 000DFFFFh†
  00800000h - 00FFFFFFh (8 Mbyte to 16 Mbyte)
  01000000h - 03FFFFFFh (16 Mbyte to 64 Mbyte)

† Indicates the default decoding

- STD 32 I/O address decoding

  Certain regions of the I/O address range can be dedicated to the STD 32 bus. IBM AT-compatible peripherals normally must be mapped within the 100h-3FFh address range. Most other I/O from Ziatech is mapped in the E000h-FFFFh range. Regions that are dedicated to the STD 32 bus cannot be used for PCI peripherals. Most PCI peripherals are configurable for addresses other than 100h-3FFh, so this should not be a problem. The following regions are configurable for STD 32 usage:

  100h - 1FFh†
  200h - 2FFh†
  300h - 3FFh†
  E000h-FFFFh†

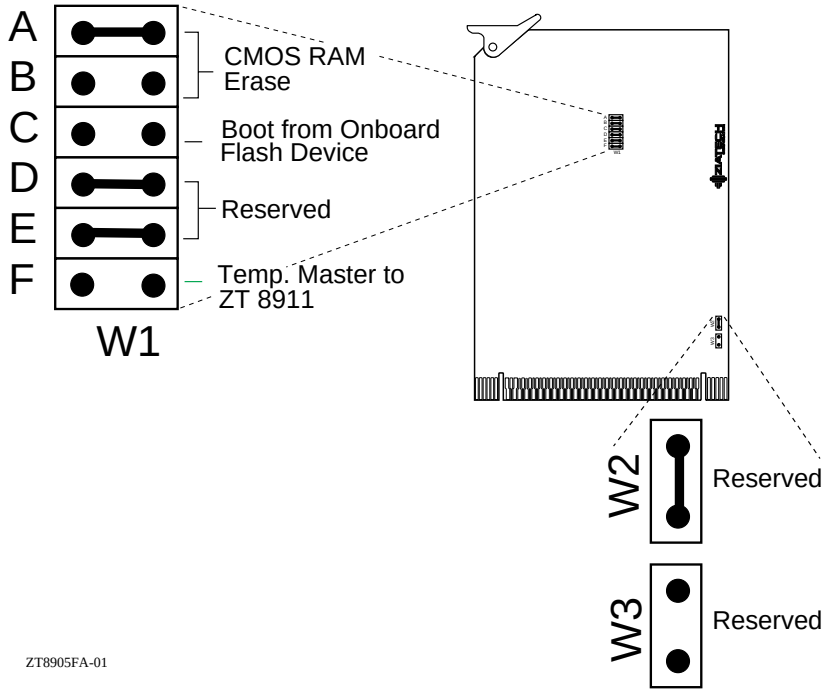
† Indicates the default decoding

JUMPER OPTIONS AND LOCATIONS

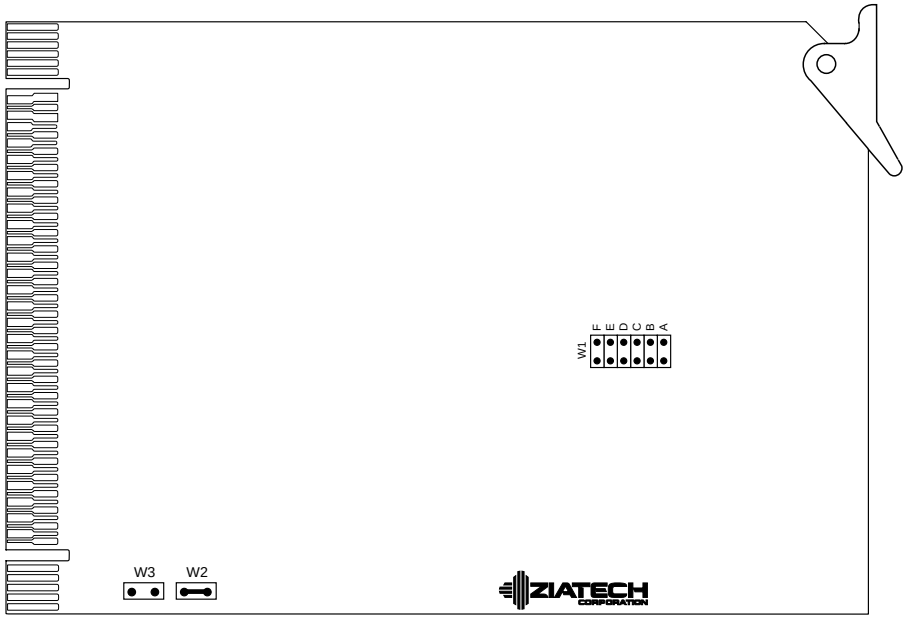
The ZT 8905 includes eight jumpers, W1A-W1F, W2, and W3. W1A-W1F are located underneath the EPROM/FLASH socket (this is the socket used for the alternate boot image). W2 and W3 are located near the gold fingers and are reserved for factory use only. W2 should always be installed and W3 removed.

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The "DOS Factory Default Jumper Configuration" illustration and the "Customer Jumper Configuration" illustration are shown below. The "Customer Jumper Configuration" illustration provides a blank jumper layout allowing you to document your jumper configuration if it differs from the factory default.



DOS Factory Default Jumper Configuration



Note: Do not remove W2 or install W3.

Customer Jumper Configuration

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JUMPER CROSS-REFERENCE TABLE

The following table divides the jumper options into functional groups. Click on any jumper number for a description of the jumper.

Function	Jumpers
CMOS RAM Erase	W1A,W1B
Boot From On-Board Flash Device	W1C
Reserved	W1D, W1E
Temp Master to ZT 8911	W1F
Reserved	W2, W3

JUMPER DESCRIPTIONS

The following topics list the jumpers in numerical order and provide a detailed description of each jumper. A dagger (†) indicates the default jumper configuration. Click on the green jumper number at the top of the topic for an illustration showing jumper locations.

W1A, W1B (CMOS RAM Erase)

W1A, W1B removes the contents of the battery backed CMOS configuration RAM. The CMOS RAM is erased by turning off the power and moving the W1A shorting jumper to position W1B and back to W1A again.

	W1A	W1B	CMOS Configuration RAM
†	IN	OUT	Normal operation
	OUT	IN	Erase

W1C (Boot From On-Board Flash Device)

W1C enables the ZT 8905 to begin program execution from the local Flash device or an alternate boot image loaded in the socket at T6C. Select the alternate boot operation if the local Flash device is corrupted and the ZT 8905 fails to boot properly. W1C must be removed when booting from a device in socket T6C.

	W1C	Boot Source
†	IN	Local Flash memory
	OUT	Alternate boot image in socket at T6C

† Factory default configuration for DOS systems

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W1D (Reserved)

Reserved. This jumper must be left installed.

W1E (Reserved)

Reserved. This jumper must be left installed.

W1F (Temporary Master to ZT 8911)

When the ZT 8905 is used in a STAR SYSTEM that has the ZT 8911 as the Permanent Master, jumper W1F must be installed. W1F controls the backplane environment to let the ZT 8911 perform system translation cycles between the ZT 8905 and SA/EA peripherals. See the "Multiple Master System Requirements" section in Chapter 3 for more information on operating the ZT 8905 in a multiple master architecture.

	W1F	Temporary Master Type
	IN	Enabled
†	OUT	Disabled

W2, W3 (Reserved)

W2 should always be installed and W3 removed (factory default).

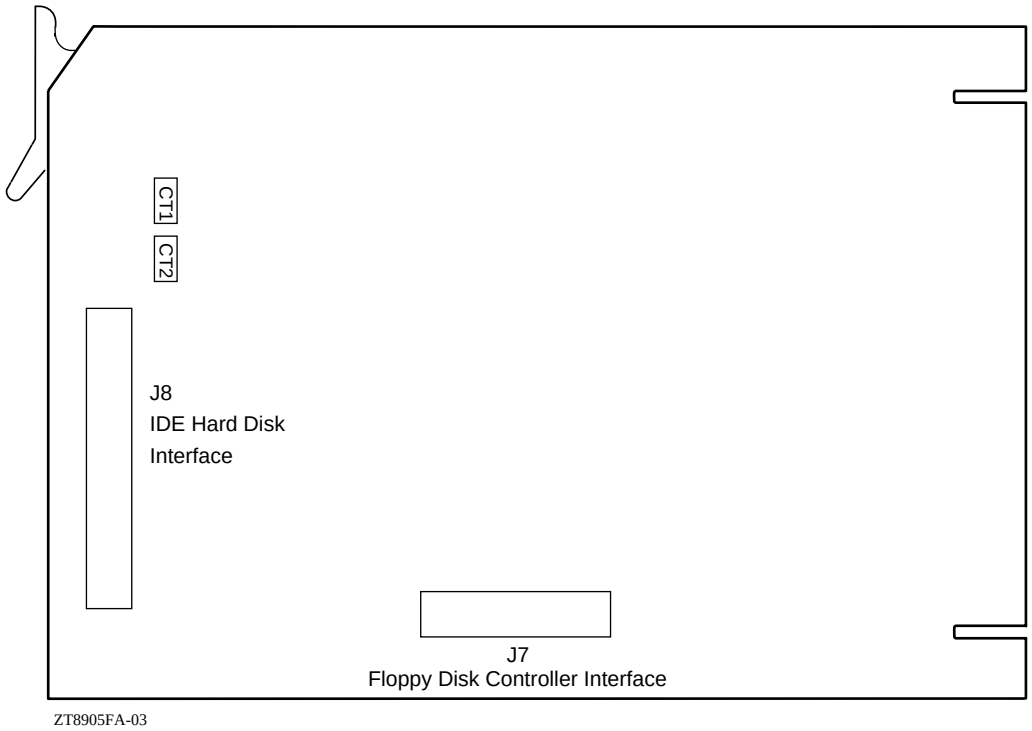
CUTTABLE TRACE OPTIONS AND LOCATIONS

The ZT 8905 supports the option of assigning up to two additional DMA channels for frontplane operation with the addition or removal of two 0 ohm surface mount resistors, CT1 and CT2. These are factory-installed options only.

A "Cuttable Trace Locations" figure and a detailed description of CT1 and CT2 are provided on the following page. A dagger (†) indicates the default configuration.

† Factory default configuration for DOS systems

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Cuttable Trace Locations

CT1, CT2 (Frontplane DMA)

CT1 and CT2 assign up to two additional DMA channels for frontplane operation.

	CT1	**Function**
	IN	Connects J5 pin 53 to DMA Channel 6 DACK*
†	OUT	No connection

	CT2	**Function**
	IN	Connects J5 pin 57 to DMA Channel 7 DACK*
†	OUT	No connection

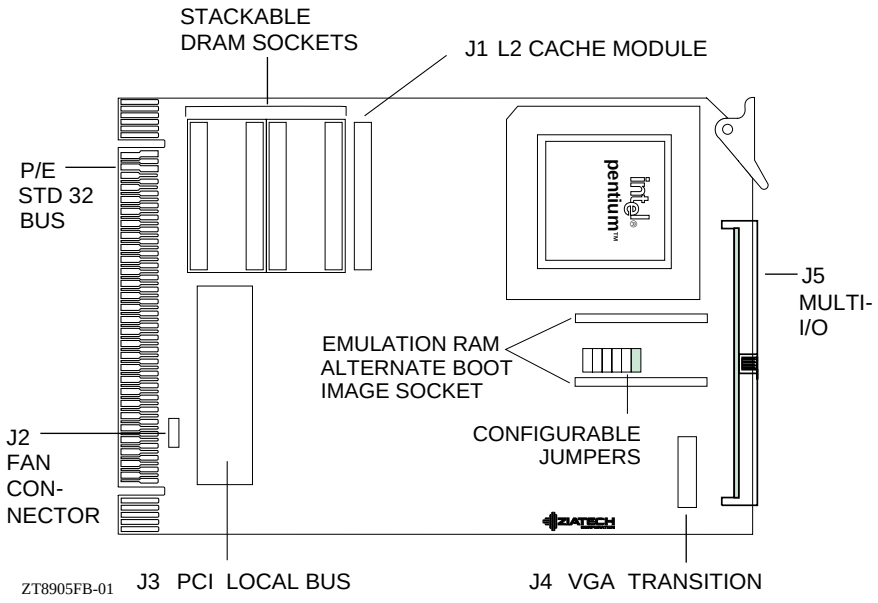
† Factory default configuration for DOS systems

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APPENDIX B. SPECIFICATIONS

This appendix describes the electrical, environmental, and mechanical specifications of the ZT 8905. It also includes illustrations of the board dimensions, the P/E connector pinouts, and the cable commonly used with the ZT 8905, as well as tables showing the pin assignments for the ZT 8905's I/O connectors. The "ZT 8905 Key Parts" figure below shows the locations of the connectors, jumpers, and sockets on the ZT 8905.



ZT 8905 Key Parts

ELECTRICAL AND ENVIRONMENTAL

The following topics list electrical and environmental specifications, including absolute maximum ratings, DC operating characteristics, battery backup characteristics, and STD bus loading characteristics.

Absolute Maximum Ratings

- Supply Voltage, Vcc: 0 to 7 V
- Supply Voltage, AUX +: 0 to 12.6 V

(required for 4 Mbyte Flash programming and fan/heatsink only; 2 Mbyte Flash operation does not require +12 V)

- Supply Voltage, AUX -: Not used
- Storage Temperature: -40° to +85° Celsius
- Non-Condensing Relative Humidity: <95% at 40° Celsius

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Operating Temperature

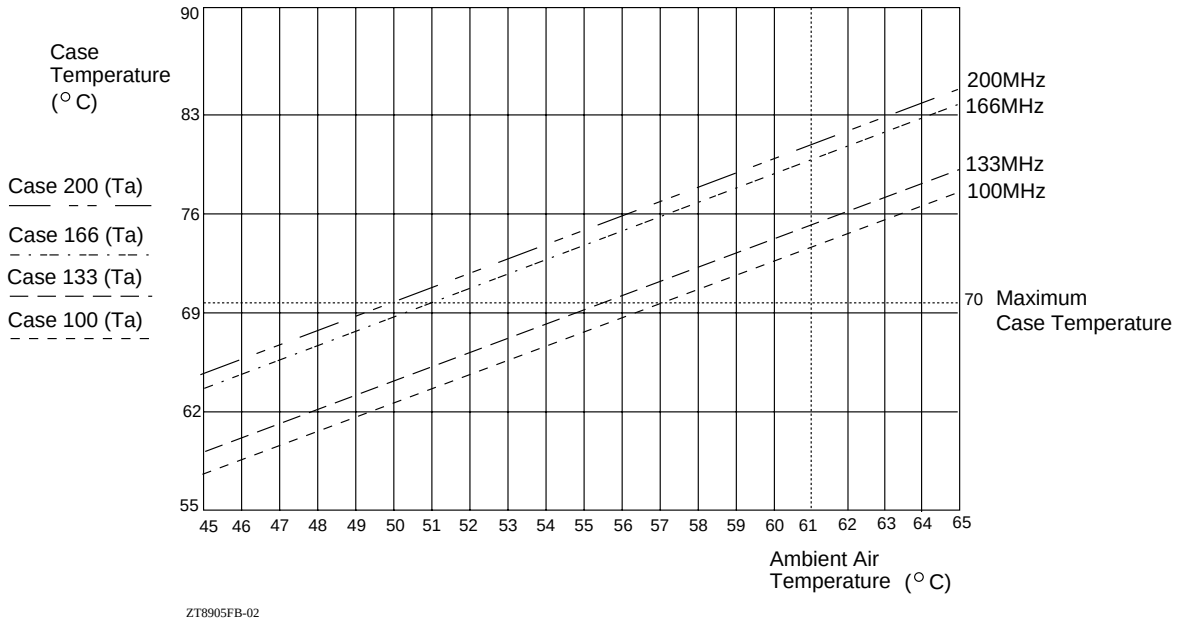
The values in the figure and table referenced below are stress ratings only. Do not operate the ZT 8905 at these maximums. See the "DC Operating Characteristics" section in this appendix for operating conditions.

For proper operation of the ZT 8905, the Pentium processor case temperature must remain below 70° Celsius. An integrated fan/heatsink is provided with the processor to help maintain this requirement.

See the "Ambient Temperature Vs. Pentium Processor Case Temperature" figure and the "Pentium Processors Maximum Ambient Temperature" table below.

Pentium Processors Maximum Ambient Temperatures

Processor Speed (MHz)	Max. Ambient Temperature (°C)
100	57.0
133	55.5
166	51.0
200	50.0



Ambient Temperature Vs. Pentium Processor Case Temperature

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DC Operating Characteristics

- Supply VoltageVcc: 4.75 to 5.25 V
- Supply Voltage, AUX +: 11.4 to 12.6 V (for 4 Mbyte Flash programming)
- Supply Voltage, AUX -: Not used
- Supply Current, Icc:

Pentium-100:	2.1 A typ., 2.9 max.	(Numbers assume 8 Mbytes of DRAM
Pentium-133:	2.3 A typ., 3.1 max.	and 2 Mbytes of Flash. Each additional
Pentium-166:	2.6 A typ., 3.5 max.	8 Mbytes adds 0.2 A typ., 0.3 A max.)
Pentium-200:	2.9 A typ., 3.8 max.	

- Supply Current, AUX + (12 V): 4 Mbyte Flash Option: 0.010 A typ., 0.015 A max.
  Fan/Heatsink: 120 mA typ., 200 mA max.

Battery Backup Characteristics

- Battery Voltage: 3 V
- Battery Capacity: 255 mAH
- Real-Time Clock Requirements: 4 µA max. (Vbat = 3 V, Vcc=0 V)
- Real-Time Clock data retention:

--In the absence of power:	56250 Hours/ 6.4 years min.
--With Vcc power applied 8 hours per day:	9.6 years min.

- Electrochemical Construction: Poly-carbonmonofluoride

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STD Bus Loading Characteristics

The unit load is a convenient method for specifying the input and output drive capability of STD bus cards. With this method, one unit load is equal to one LSTTL load as follows:

- Current for single input load: 20 µA
- Current for single output drive: 400 µA

The unit load reflects current requirements at worst case conditions over the recommended supply voltage and operating temperature ranges. An output drive of 60 unit loads drives 60 STD bus cards having input ratings of one unit load. The "STD Bus Loading, P Connector" table includes load values for STD-80 connections. The "STD Bus Loading, E Connector" table includes load values for STD 32 connections.

STD Bus Loading, P Connector

PIN (CIRCUIT SIDE)							PIN (COMPONENT SIDE)
OUTPUT DRIVE							OUTPUT DRIVE
INPUT LOAD							INPUT LOAD
MNEMONIC							MNEMONIC
+5 VDC	REQ		P2	P1		REQ	+5 VDC
GND	REQ		P4	P3		REQ	GND
DCPDN*	1	40	P6	P5			VBAT
D7/A13 [1]	3	53	P8	P7	53	3	D3/A19 [1]
D6/A22 [1]	3	53	P10	P9	53	3	D2/A18 [1]
D5/A21 [1]	3	53	P12	P11	53	3	D1/A17 [1]
D4/A20 [1]	3	53	P14	P13	53	3	D0/A16 [1]
A15	1	55	P16	P15	55	1	A7
A14	1	55	P18	P17	55	1	A6
A13	1	55	P20	P19	55	1	A5
A12	1	55	P22	P21	55	1	A4
A11	1	55	P24	P23	55	1	A3
A10	1	55	P26	P25	55	1	A2
A9	1	55	P28	P27	55	1	A1
A8	1	55	P30	P29	55	1	A0
RD*	1	55	P32	P31	55	1	WR*
MEMRQ*	1	55	P34	P33	55	1	IORQ*
BHE	1	55	P36	P35	55	1	IOEXP
ALE*	1	55	P38	P37	55	1	INTRQ1*
STATUS 0*	1	55	P40	P39	55	1	STATUS 1*
BUSRQ*	1	55	P42	P41	55	1	BUSAK*
INTRQ*	1		P44	P43			INTAK*
NMIRQ*	1		P46	P45		1	WAITRQ*
PBRESET*	1		P48	P47	55	1	SYSRESET*
INTRQ2* (CNTRL*)	1		P50	P49	52	3	CLOCK*
PCI [2]	1		P52	P51			PCO [2]
AUX GND	REQ		P54	P53		REQ	AUX GND
AUX-V			P56	P55		REQ	AUX+V

Notes:
REQ indicates required connection.
[1] High order address bits multiplexed over data bus.
[2] PCI connected to PCO.

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STD Bus Loading, E Connector

PIN (CIRCUIT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC							PIN (COMPONENT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC
LOCK*	1	55	E2	E1		REQ	GND
XA23	1	55	E4	E3	55	1	XA19
XA22	1	55	E6	E5	55	1	XA18
XA21	1	55	E8	E7	55	1	XA17
XA20	1	55	E10	E9	55	1	XA16
RSVD			E12	E11	55	1	NOWS*
+5 VDC	REQ		E14	E13		REQ	+5 VDC
DREQx*			E16	E15	55		DAKx*
GND	REQ		E18	E17		REQ	GND
D31	1		E20	E19	55	1	D27
D30	1		E22	E21	55	1	D26
D29	1		E24	E23	55	1	D25
D28	1		E26	E25	55	1	D24
GND	REQ		E28	E27	55	1	D23
D15	1	55	E30	E29	55	1	D22
D14	1	55	E32	E31	55	1	D21
D13	1	55	E34	E33	55	1	D20
D12	1	55	E36	E35		REQ	GND
D11	1	55	E38	E37	55	1	D19
D10	1	55	E40	E39	55	1	D18
D9	1	55	E42	E41		1	D17
D8	1	55	E44	E43		1	D16
MASTER16*	1	55	E46	E45		REQ	GND
AENx*		55	E48	E47			IRQx
BE3*	1	55	E50	E49	55	1	BE1*
BE2*	1	55	E52	E51	55	1	BE0*
GND	REQ		E54	E53	55	1	MEM16*
W-R	1	55	E56	E55	55	1	M-IO
DMAIOR*	1	55	E58	E57	55	1	DMAIOW*
EX8*	1		E60	E59		1	IO16*
START*	1	55	E62	E61	55	1	CMD*
EX32*	1		E64	E63		1	EX16*
T-C	1		E66	E65		1	EXRDY
+5 VDC	REQ		E68	E67		1	INTRQ3*
MREQx*		55	E70	E69		1	MAKx*
MSBURST*		55	E72	E71		1	SLBURST*
XA31*	1	55	E74	E73	55	1	XA27*
XA30*	1	55	E76	E75	55	1	XA26*
XA29*	1	55	E78	E77	55	1	XA25*
XA28*	1	55	E80	E79	55	1	XA24*

Note:
REQ indicates required connection.

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MECHANICAL

The following topics list mechanical specifications, including card dimensions and weight, connectors, and cables.

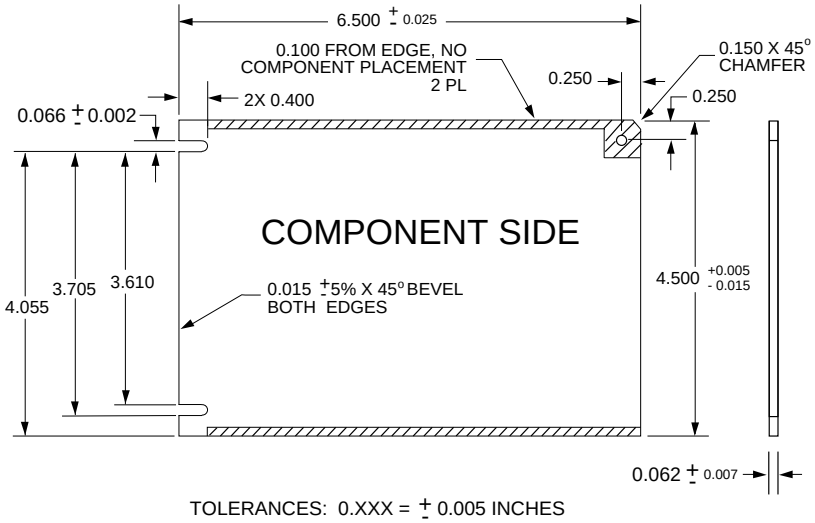
Card Dimensions and Weight

The ZT 8905 meets the *STD 32 Bus Specification and Designer's Guide* for all mechanical parameters. In a card cage with 0.625 inch spacing, the ZT 8905 requires two card slots with the integrated fan/heatsink. An additional card slot is required for the optional IDE interface (D1 option).

Mechanical dimensions are shown in the "Board Dimensions" illustration and are outlined below.

- Board Length: 16.51±0.063 cm (6.500 ±0.025 inches)
- Board Width: 11.43±0.038 cm (4.500 ±0.015 inches)
- Board Thickness: 0.158 ±0.018 cm (0.062 ±0.007 inches)
- Board Weight:
  - --Without heatsink/fan: 212 grams (7.5 ounces)
  - --With heatsink/fan: 255 grams (9 ounces)
  - --ZT 8906: 1.004 Kilograms (2 lbs 3.4 ounces) (including 3-slot CompactPCI enclosure)
- Board Height:
  - --From top surface: 2.54 cm (1 inch)
  - --From bottom surface: 0.12 cm (0.047 inches)

The ZT 8906, with its CompactPCI enclosure, occupies a total of six STD 32 card slots, allowing three CompactPCI peripherals to be used inside an STD 32 card cage.



Board Dimensions

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Connectors

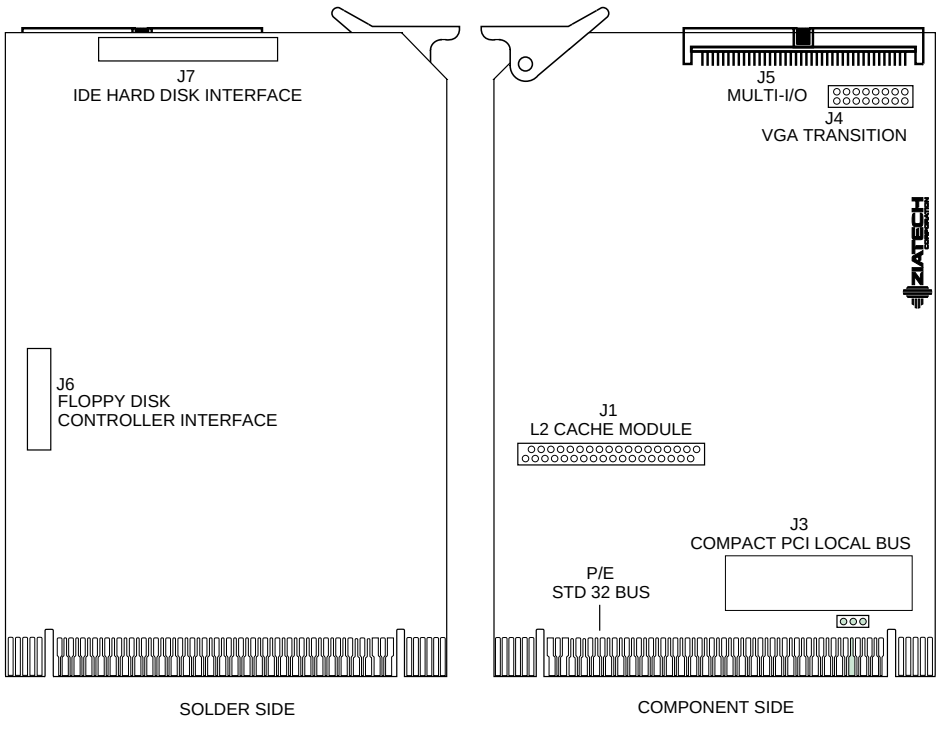
As shown in the "Connector Locations" illustration, the ZT 8905 includes several connectors to interface to the STD bus and application-specific devices. The topics that follow provide descriptions of the individual connectors. Connector assignments are listed below.

Please note the revision of the ZT 8905 that you are using. The table below is for boards that are Revision A and higher, which have different connector assignments than the Revision 0 board. Customers with Revision 0 boards should refer to the Revision 0 manual for connector and cabling information.

Connector Assignments

ZT 8905 Boards Revision A and Higher

Connector	Function
J1	Optional L2 cache module
J2	Fan Connector Location
J3	PCI local bus interface
J4	VGA transition connector
J5	Multi-I/O connector including DMA, Interrupts
J6	Floppy disk controller interface (OEM Option)
J7	IDE hard disk interface

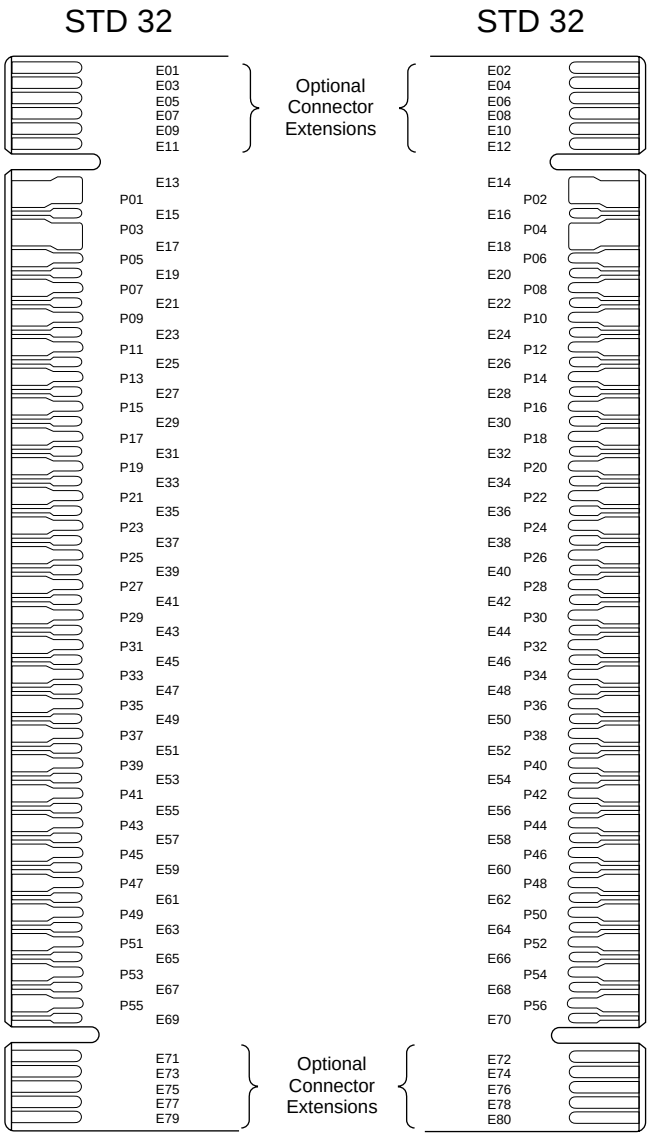


Connector Locations

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P/E (STD-80/STD 32 Bus)

The E connector interfaces the ZT 8905 to the STD 32 bus. This connector combines the STD-80 interface (on the P pins) with the additional signals defined for STD 32 (on the E pins) to make a 136-pin (dual 68-pin) card-edge connector with fingers on 0.0625 inch contact spacing. The mating connector is a Viking S3VT68/5DP12 or equivalent for the solder tail, or a Viking S3VT68/5DE12 or equivalent for the card extender. The pin assignments for the P/E connector are shown in the "P/E Connector Pinout" illustration below and in the STD bus loading tables.



P/E Connector

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J1 (L2 Cache Module)

J1 is a 36-pin location for an optional L2 cache module. Contact Ziatech for availability.

J2 (Fan Connector)

J2 is a 3-pin vertical male header with 0.1 inch contact spacing for supplying power to the fan/heatsink. +12 V is used to power the fan. Pin 2 is an optional Tachometer input from fans so equipped. The pin assignments are given in the "J2 Fan Connector Pinout" table below.

J2 Fan Connector Pinout

Pin #	Signal	Type	Description
1	+12V	Power	+12V For fan
2	TACH IN	In	Tach Input (Option)
3	GND	Ground	Ground

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J3 (PCI Local Bus Interface)

J3 is a 175-pin 2 mm x 2 mm female receptacle providing the PCI local bus interface to optional mezzanine adapters designed for this application. J3 provides a complete 32-bit PCI interface. This connector is CompactPCI compatible. Refer to the *CompactPCI Specification* for details. Do not use Revision 0.x zPM10 VGA modules on Revision A or higher ZT 8905 boards. The pin assignments are given in the "J3 PCI Local Bus Connector Pinout" table below.

J3 PCI Local Bus Connector Pinout

(For Revision A Boards and Higher)

Pin #	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	BRSV	3.3V	5V	GND
24	GND	AD[1]	5V	5V	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	GND	C/BE[0]#	GND
20	GND	AD[12]	GND	5V	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND
16	GND	DEVSEL#	GND	5V	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
14	GND	CLK13	GND	REQ4#	CLK13	GNT4#	GND
13	GND	GNT2#	CLK02	REQ3#	GND	GNT3#	GND
12	GND	REQ1#	GND	GNT1#	CLK13	REQ2#	GND
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	5V	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK02	AD[31]	GND
5	GND	BRSV	BRSV	RST#	GND	GNT#	GND
4	GND	BRSV	GND	5V	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

Notes:

1. The above pinout is for Revision A boards. Previous revisions of the ZT 8905 have a modified pinout that is NOT COMPATIBLE with Revision A.
2. Rows 12-14 are not for adapter use. Adapters use pin D6 for CLK, pin A6 for REQ#, and pin E5 for GNT#.
3. Column 2 is unused in mezzanine applications.

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J4 (VGA Transition Connector)

J4 provides an interface for optional PCI VGA Interface boards to pass down the video signals to the ZT 8905 for routing through the J5 multi-I/O connector interface. This mechanism allows all cabling to be done through J5, including the VGA interface. The zPM10 Super VGA Interface uses this mechanism. The pin assignments are given in the "J4 VGA Transition Connector Pinout" table below.

J4 VGA Transition Connector Pinout

Pin #	Signal	Type	Description
1	RED	Out	VGA Red
2	GRN	Out	VGA Green
3	BLUE	Out	VGA Blue
4	OPT1	------	VGA Opt1
5	GND	------	Ground (Dig)
6	GND	------	Ground (Red)
7	GND	------	Ground (Green)
8	GND	------	Ground (Blue)
9	VCC	------	+5V (Option)
10	GND	------	Ground (Sync)
11	OPT2	------	VGA Opt2
12	SDA	In/Out	VGA Data
13	HSYNC	Out	VGA Hor. Sync.
14	VSYNC	Out	VGA Ver. Sync.
15	SCL	Out	VGA Data Clock
16	NC	------	No Connect

J5 (Multi-I/O Connector)

J5 is a multi-I/O connector that provides a high density connection to the following interfaces:

- COM1
- COM2
- VGA (if PCI VGA interface loaded)
- Local Keyboard
- LPT1
- External LED
- External Push-button Reset switch
- DMA
- Interrupts

The pin assignments for the J5 connector are given in the "J5 Multi-I/O Connector Pinout" table on the following page.

Ziatech offers the ZT 90205 transition cable that breaks out these signals into standard D-SHELL 0.1" connector interfaces. This cable is documented at the end of this appendix.

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J5 Multi-I/O Connector Pinout

	Description	Type	Signal	Pin #	Pin #	Signal	Type	Description	
FRONTPLANE INTERRUPT	Ground	------	GND	1	51	DRQ6*	In	DMA Request 6	FRONTPLANE DMA
	Configurable	In	FP1*	2	52	DRQ1*	In	DMA Request 1	
	Ground	------	GND	3	53	DAK6*	Out	DMA Acknowledge 6	
	Configurable	In	FP3*	4	54	DAK1*	Out	DMA Acknowledge 1	
	Ground	------	GND	5	55	DRQ7*	In	DMA Request 7	
	Interrupt Level 10	In	FP5*	6	56	DMAIOW*	Out	I/O Write	
	Ground	------	GND	7	57	DAK7*	Out	DMA Acknowledge 7	
	Interrupt Level 11	In	FP6*	8	58	DMAIOR*	Out	I/O Read	
	Ground	------	GND	9	59	GND	------	Ground	
	Interrupt Level 12	In	FP7*	10	60	TC*	Out	Terminal Count	
COM 1	COM1 DCD	In	DCD	11	61	STB*	Out	Data strobe	IEEE 1284 PORT
	COM1 DSR	In	DSR	12	62	AFD*	Out	Autofeed	
	COM1 RXD	In	RxD	13	63	PD0	In/Out	Data bit 0	
	COM1 RTS	Out	RTS	14	64	ERR*	In	Error	
	COM1 TxD	Out	TxD	15	65	PD1	In/Out	Data bit 1	
	COM1 CTS	In	CTS	16	66	INIT*	Out	Initialize	
	COM1 DTR	Out	DTR	17	67	PD2	In/Out	Data bit 2	
	COM1 RINGIN	In	RIN	18	68	SLIN*	Out	Select to printer	
	Ground	------	GND	19	69	PD3	In/Out	Data bit 3	
	+5V (Fused)	------	VCC	20	70	GND	------	Ground	
COM 2	COM2 DCD	In	DCD	21	71	PD4	In/Out	Data bit 4	
	COM2 DSR	In	DSR	22	72	GND	------	Ground	
	COM2 RXD	In	RxD	23	73	PD5	In/Out	Data bit 5	
	COM2 RTS	Out	RTS	24	74	GND	------	Ground	
	COM2 TxD	Out	TxD	25	75	PD6	In/Out	Data bit 6	
	COM2 CTS	In	CTS	26	76	GND	------	Ground	
	COM2 DTR	Out	DTR	27	77	PD7	In/Out	Data bit 7	
	COM2 RINGIN	In	RIN	28	78	GND	------	Ground	
	Ground	------	GND	29	79	ACK*	In	Acknowledge	
	+5V (Fused)	------	VCC	30	80	GND	------	Ground	
VGA	VGA Red	Out	RED	31	81	BUSY	In	Printer busy	
	VGA Green	Out	GRN	32	82	GND	------	Ground	
	VGA Blue	Out	BLUE	33	83	PE	In	Paper error	
	VGA Opt1	------	OPT1	34	84	GND	------	Ground	
	Ground (Dig)	------	GND	35	85	SLCT	In	Select from printer	
	Ground (Red)	------	GND	36	86	VCC	------	+5VLED (620 ohm)	LED
	Ground (Green)	------	GND	37	87	FPLED	Out	LED drive control	
	Ground (Blue)	------	GND	38	88	VCC	------	+5V (Fused)	SPK
	+5V (Option)	------	VCC	39	89	FPSPK	Out	Speaker control	
	Ground (Sync)	------	GND	40	90	RSVD	------	Factory Reserved	RESERVED
	VGA Opt2	------	OPT2	41	91	RSVD	------	Factory Reserved	
	VGA Data	In/Out	SDA	42	92	RSVD	------	Factory Reserved	
	VGA Hor. Sync.	Out	HSYNC	43	93	RSVD	------	Factory Reserved	
	VGA Ver. Sync.	Out	VSYNC	44	94	RSVD	------	Factory Reserved	
	VGA Data Clock	Out	SCL	45	95	RSVD	------	Factory Reserved	
KEY	+5V (Fused)	------	VCC	46	96	RSVD	------	Factory Reserved	
	Keyboard Clock	In/Out	KCLK	47	97	RSVD	------	Factory Reserved	
	Ground	------	GND	48	98	RSVD	------	Factory Reserved	
	Keyboard Data	In/Out	KDAT	49	99	RSVD	------	Factory Reserved	
R	PBReset	In	PBR	50	100	RSVD	------	Factory Reserved	

ZT8905TB-09

Notes: Pins labeled as Factory Reserved MUST NOT BE CONNECTED in user applications. These signals are used for diagnostic and configuration of the ZT 8905 during test.

The TYPE of signal is referenced to the ZT 8905. Out signals are signals the ZT 8905 drives, In signals are signals that the ZT 8905 receives.

The interrupt levels shown are the most common configuration. Refer to the "Interrupt Architecture" figure in Chapter 4, "Interrupt Controller," for other possibilities.

The frontplane interrupts are active low inputs that are routed through an inverter before being applied to the interrupt controller. Pins 2 and 4 are configurable through the BIOS SETUP Utility: Screen 2.

Pin 53 and pin 57 may optionally be disconnected through 0 Ω resistors at CT1 and CT2.

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J6 (Floppy Disk Controller Interface)

J6 is a surface mount connector location for an optional floppy disk controller interface. Contact Ziatech for details. This interface is provided primarily for single board computer operation (without an STD 32 backplane). STD 32 users should use the ZT 8954 Floppy Disk Controller Interface for floppy support.

J7 (IDE Hard Disk Interface)

J7 is a 44-pin surface mount connector location to provide a local Integrated Drive Electronics (IDE) hard disk interface. The pin assignments are given in the "J7 IDE Hard Disk Connector Pinout" table below. The ZT 8905 can, as an option, have an IDE drive integrated with it (ordering option D1). This option is useful for single board computer operation (no STD 32 backplane) or for STAR SYSTEM operation where the hard disk interface is local to the ZT 8905.

J7 IDE Hard Disk Connector Pinout

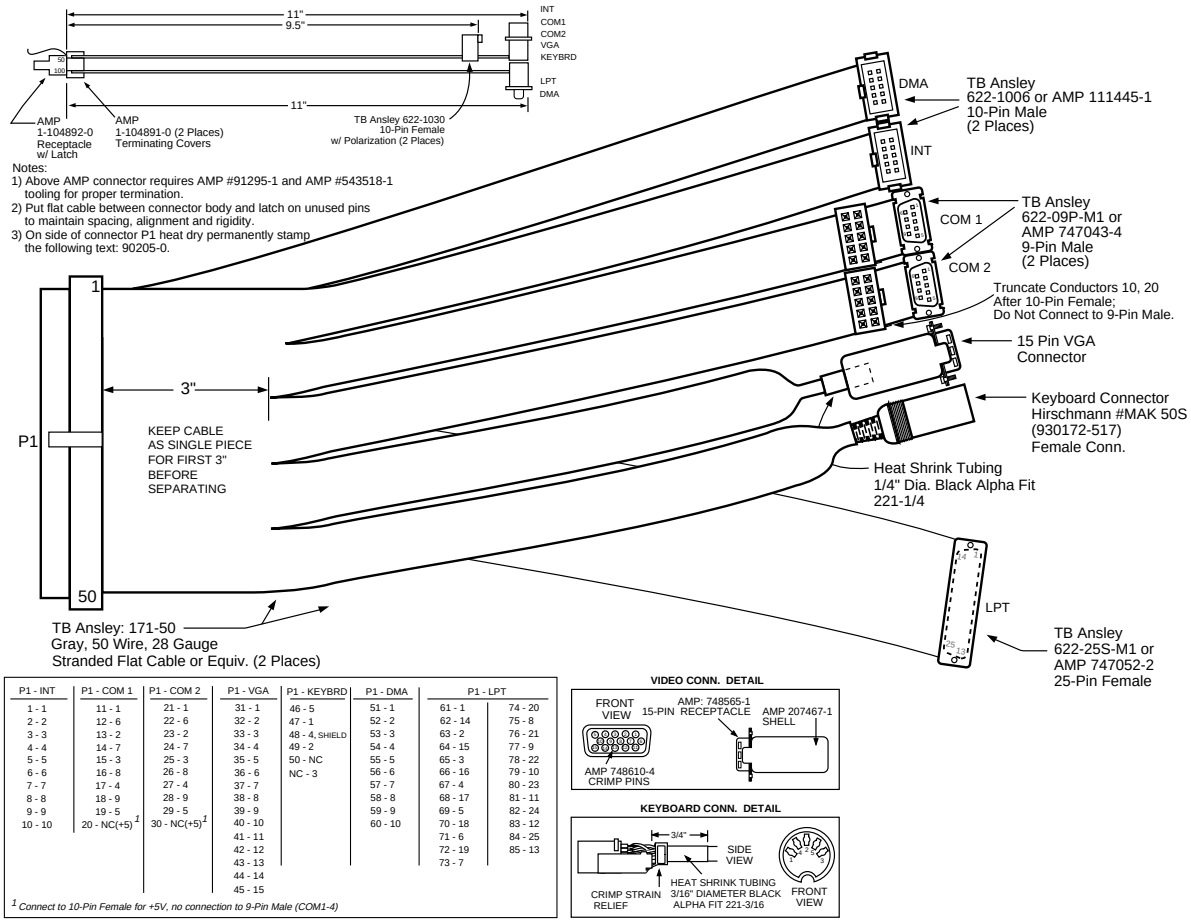
Pin #	Signal	Type	Description	Pin #	Signal	Type	Description
1	RESET*	Out	Reset	23	IOWR*	Out	I/O Write Strobe
2	GND	------	Ground	24	GND	------	Ground
3	D7	In/Out	Data Bit 7	25	IORD*	Out	I/O Read Strobe
4	D8	In/Out	Data Bit 8	26	GND	------	Ground
5	D6	In/Out	Data Bit 6	27	RSVD	------	Reserved (IORDY)
6	D9	In/Out	Data Bit 9	28	ALE	Out	Address Latch En.
7	D5	In/Out	Data Bit 5	29	RSVD	------	Reserved
8	D10	In/Out	Data Bit 10	30	GND	------	Ground
9	D4	In/Out	Data Bit 4	31	IRQ	In	Interrupt Request
10	D11	In/Out	Data Bit 11	32	IOCS16*	In	16-bit I/O handshake
11	D3	In/Out	Data Bit 3	33	A1	Out	Address Bit 1
12	D12	In/Out	Data Bit 12	34	PDIAG	------	Inter-drive diagnostics
13	D2	In/Out	Data Bit 2	35	A0	Out	Address Bit 0
14	D13	In/Out	Data Bit 13	36	A2	Out	Address Bit 2
15	D1	In/Out	Data Bit 1	37	CS0*	Out	Chip Select (1F0h-1FFh)
16	D14	In/Out	Data Bit 14	38	CS1*	Out	Chip Select (3F6h)
17	D0	In/Out	Data Bit 0	39	ACT*	In	Active/Slave present
18	D15	In/Out	Data Bit 15	40	GND	------	Ground
19	GND	------		41	VCC	------	+5V - Drive Logic
20	KEY	------	Cable Key	42	VCC	------	+5V - Drive Motor
21	RSVD	------	Reserved	43	GND	------	Ground
22	GND	------	Ground	44	XT/AT	Out	Drive Mode = AT

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Cable

The following cable is available from Ziatech Corporation. A drawing is included here as reference for those who wish to make their own cable:

ZT 90205 Multi-I/O cable supports VGA, keyboard, COM1, COM2, LPT1, DMA, and Interrupts through J5. The speaker interface is not supported with this cable.



P1 - INT	P1 - COM 1	P1 - COM 2	P1 - VGA	P1 - KEYBRD	P1 - DMA	P1 - LPT	
1 - 1	11 - 1	21 - 1	31 - 1	46 - 5	51 - 1	61 - 1	74 - 20
2 - 2	12 - 6	22 - 6	32 - 2	47 - 1	52 - 2	62 - 14	75 - 8
3 - 3	13 - 2	23 - 2	33 - 3	48 - 4, SHIELD	53 - 3	63 - 2	76 - 21
4 - 4	14 - 7	24 - 7	34 - 4	49 - 2	54 - 4	64 - 15	77 - 9
5 - 5	15 - 3	25 - 3	35 - 5	50 - NC	55 - 5	65 - 3	78 - 22
6 - 6	16 - 8	26 - 8	36 - 6	NC - 3	56 - 6	66 - 16	79 - 10
7 - 7	17 - 4	27 - 4	37 - 7		57 - 7	67 - 4	80 - 23
8 - 8	18 - 9	28 - 9	38 - 8		58 - 8	68 - 17	81 - 11
9 - 9	19 - 5	29 - 5	39 - 9		59 - 9	69 - 5	82 - 24
10 - 10	20 - NC(+5) [1]	30 - NC(+5) [1]	40 - 10		60 - 10	70 - 18	83 - 12
			41 - 11			71 - 6	84 - 25
			42 - 12			72 - 19	85 - 13
			43 - 13			73 - 7	
			44 - 14				
			45 - 15				

[1] *Connect to 10-Pin Female for +5V, no connection to 9-Pin Male (COM1-4)*

ZT 90205 Rev. 0 Multi-I/O Cable

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APPENDIX C. CUSTOMER SUPPORT

This appendix offers technical assistance information for this product, and also the necessary information should you need to return a Ziatech product.

TECHNICAL/SALES ASSISTANCE

If you have a technical question, please call Ziatech's Customer Support Service at one of the numbers below, or e-mail our technical support team at **tech_support@ziatech.com**.

If you have a sales question, please contact your local Ziatech Sales Representative or the Regional Sales Office for your area.

Additional information is available at Ziatech's website, located at **http://www.ziatech.com**.

Corporate Headquarters
1050 Southwood Drive
San Luis Obispo, CA 93401 USA
Tel (805) 541-0488
FAX (805) 541-5088

Central Regional Office
7700 Chevy Chase Drive, Suite 110-A
Austin, TX 78752 USA
Tel (512) 458-3177
FAX (512) 458-3178

Eastern Regional Office
319 North Pottstown Pike, Suite 107
Exton, PA 19341 USA
Tel (610) 524-9070
FAX (610) 524-9072

European Office
P.O Box 110
AC SON
Netherlands 5690
Tel 31-49-9460706
FAX 31-49-9460737

REVISION HISTORY

ZT 8905

Revision 0 - 2/22/95

The ZT 8905 was released to beta testing at Revision 0.

Revision A - 7/20/95

Revision A is the first production release of the ZT 8905 board.

Revision A.1 - 5/3/96

There are no functional changes between Revision A and Revision A.1.

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Revision A.2 - 11/11/96

There are no functional changes between Revision A.1 and Revision A.2. Modifications to the Revision A.2 product include:

- I/O Map was changed to decode 8000h-FFFFh to STD 32

Revision A.3 - 6/17/97

There are no functional changes between Revision A.2 and Revision A.3. Modifications to the Revision A.3 product include:

- Frontplane DMA signal routing was corrected

- Accessing I/O in the address ranges of 500-7FFh and 900-FFFh now go off-board to the STD backplane/system

ZT 8906

Revision A - 3/22/96

Revision A is the first production release of the ZT 8906 board.

Revision A.1 - 5/3/96

There are no functional changes between Revision A and Revision A.1.

Revision A.3 - 6/17/97

There are no functional changes between Revision A.2 and Revision A.3. Modifications to the Revision A.3 product include:

- Frontplane DMA signal routing was corrected

- Accessing I/O in the address ranges of 500-7FFh and 900-FFFh now go off-board to the STD backplane/system

RELIABILITY

Ziatech has taken extra care in the product design to ensure reliability. The three major ways in which reliability is achieved are:

1. The product is designed in top-down fashion, utilizing the latest in hardware and software techniques, so unwanted side effects and unclean interactions between parts of the system are eliminated.

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2. Ziatech tests each board by exercising its functions, burns it in under power, and retests it to ensure that the infant mortality phase is passed before the product is shipped.

3. Ziatech maintains a lifetime data base on each board. Any negative trends in reliability are spotted and Ziatech's suppliers are informed and/or changed.

RETURNING FOR SERVICE

Before returning any of Ziatech's products, you must phone Ziatech at (805) 541-0488 and obtain a Returned Material Authorization (RMA) number. The following information is needed to expedite the shipment of a replacement to you:

1. Your company name and address for invoice
2. Shipping address and phone number
3. Product I.D. number
4. If possible, the name of a technically qualified individual at your company familiar with the mode of failure on the board

If the unit is out of warranty, service is available at a predesignated service charge. Contact Ziatech for pricing and please supply a purchase order number for invoicing the repair.

Pack the IEEE 488 board in **anti-static** material and ship in a sturdy cardboard box with enough packing material to adequately cushion it. ***Any product returned to Ziatech improperly packed will immediately void the warranty for that particular product!*** Mark the RMA number clearly on the outside of the box before returning.

ZIATECH 5+5 WARRANTY

Ziatech provides a five-year limited warranty to its customers with a special extended warranty option. Ziatech also has an explicit policy regarding the use of Ziatech products in life support systems. These topics are covered in the following sections.

Five-Year Limited Warranty

Products manufactured by Ziatech Corporation are covered from the date of purchase by a five-year warranty against defects in materials, workmanship, and published specifications applicable to the date of manufacture. During the warranty period, Ziatech will repair or replace, solely at its option, defective units provided they are returned at customer expense to an authorized Ziatech repair facility. Products which have been subjected to misuse, abuse, neglect, alteration, or unauthorized repair, determined at the sole discretion of Ziatech, whether by accident or otherwise, are excluded from warranty. The warranty on fans and disk drives is limited to two years and the warranty on flat panel displays is limited to nine months from date of purchase. Other products and accessories not manufactured by Ziatech are limited to the warranty provided by the original manufacturer. Consumable items (fuses, batteries, etc.) and software are not covered by this warranty. Within 90 days of shipping date, Ziatech will replace software disk media should it prove defective.

Ziatech may offer, where applicable and available, replacement products; otherwise, repairs requiring components, assemblies, and other purchased materials may be limited by market availability.

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Ziatech assumes no liability resulting from changes to government regulations affecting use of materials, equipment, safety, and methods of repair. Ziatech may, at its discretion, offer replacement products.

THE ABOVE WARRANTY IS IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING, BUT NOT LIMITED TO, ANY WARRANTY FOR FITNESS OF PURPOSE, MERCHANTABILITY, OR FREEDOM FROM INFRINGEMENT OR THE LIKE, AND ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATIONS, OR SAMPLE.

Ziatech neither assumes nor authorizes any person to assume for it any other liability. The liability of Ziatech under this warranty agreement is limited to a refund of the purchase price. In no event shall Ziatech be liable for loss of profits, use, incidental, consequential, or other damage, under this agreement.

Special Extended Warranty Option

In addition to the standard five-year warranty, Ziatech offers, for a nominal fee, an extended period of warranty up to five extra years. This extended warranty period provides similar coverage and conditions as stated above in the five-year limited warranty agreement.

Life Support Policy

Ziatech products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Ziatech Corporation. As used herein:

1. Life support devices or systems are devices or systems which support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be expected to cause the failure of the life support device or system, affect its safety, or limit its effectiveness.

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APPENDIX D. PCI CONFIGURATION SPACE MAP

All PCI compliant devices contain a PCI configuration header. The generic layout of the header is shown in the "PCI Configuration Header" diagram on the following page.

Additionally, a device may contain unique configuration registers (at location > 40h). For the ZT 8905, these are shown in the "ZT 8905 On-Board Device PCI Bus Mapping" table shown below.

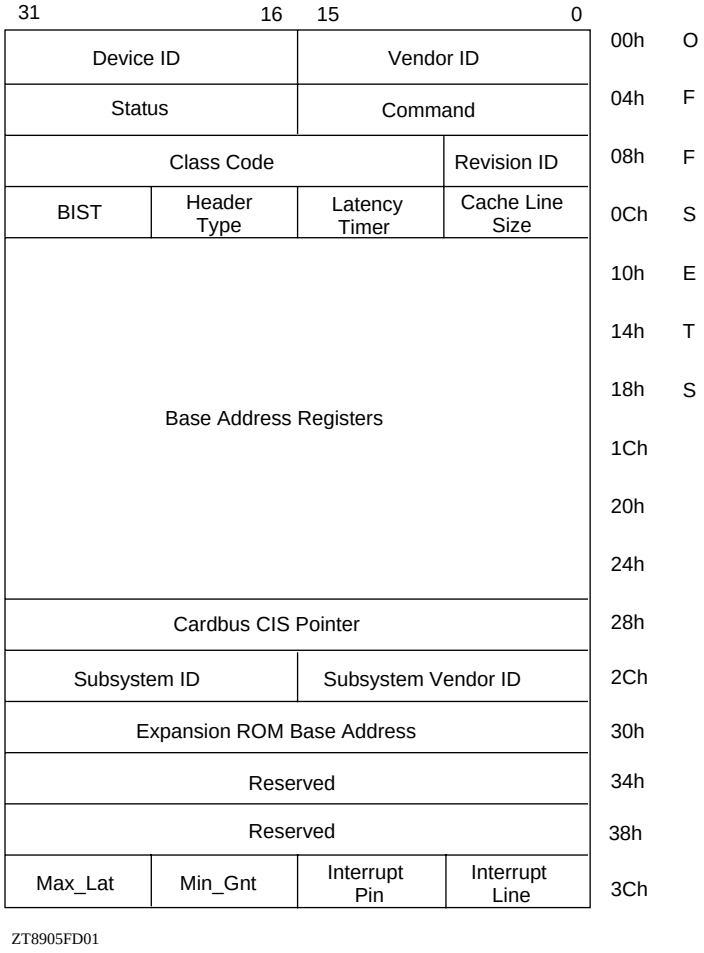
Details for each device's configuration space can be found in the respective manufacturer's data manuals. For more information on the PCI chipset implemented on the ZT 8905, refer to the *Aladdin™ M1461/M1449 3.3-Volt Pentium Chip Set Preliminary Data Sheet, Rev. D*, or contact **ALI® Pacific Technology Group** at (408) 764-0644.

ZT 8905 On-Board Device PCI Bus Mapping

Bus # (hex)	Dev # (hex)	Fcn # (hex)	Vendor ID	Device ID	Description
00	00	00	10B9	1461	Aladdin M1461 Memory Controller
00	01	00	1138	8905	Ziatech PCI-to-STD Bridge
00	02	00	10B9	1449	Aladdin M1449 PCI-to-ISA Bridge
00	03	00	†	†	Mezzanine Connector

† The vendor and device ID will vary depending upon the device plugged into the mezzanine connector.

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PCI Configuration Header

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ZIATECH CORPORATION 1050 Southwood Drive • San Luis Obispo, CA 93401 USA • Tel (805) 541-0488 • FAX (805) 541-5088

Central Regional Office
7700 Chevy Chase Drive, Suite 110-A
Austin, TX 78752 USA
Tel (512) 458-3177
FAX (512) 458-3178

Eastern Regional Office
319 North Pottstown Pike, Suite 107
Exton, Pennsylvania 19341 USA
Tel (610) 524-9070
FAX (610) 524-9072

European Office
P.O. Box 110
AC SON
Netherlands 5690
Tel 31-49-9460706
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