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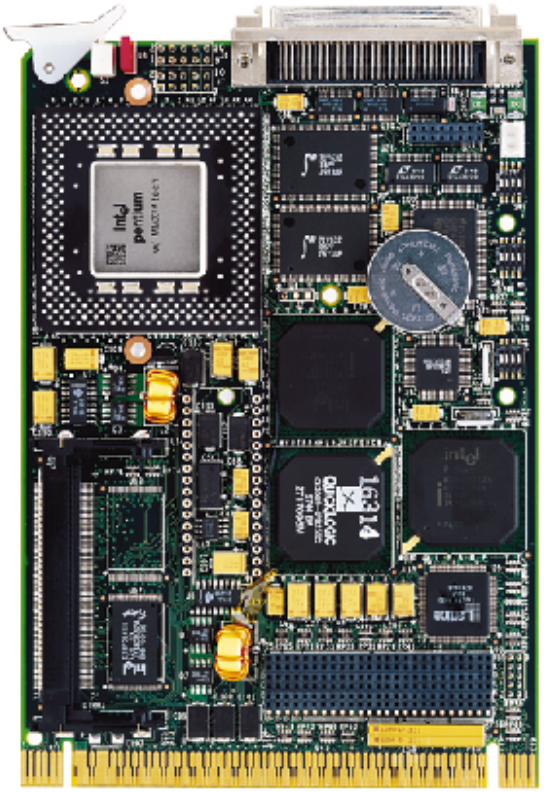
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ZT 8908



Single Board Computer with
AMD™-K6 or Pentium® Processor

Hardware User Manual

ZIATECH CORPORATION

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MANUAL ORGANIZATION

This manual describes the operation and use of the ZT 8908 Single Board Computer with AMD™-K6 or Pentium® Processor. The following summarizes the focus of each major section in this manual.

Chapter 1, "Introduction," introduces the key features of the ZT 8908. It includes a product definition, a list of product features, a functional block diagram, and a brief description of each block. This chapter is most useful to those who wish to compare the features of the ZT 8908 against the needs of a specific application.

Chapter 2, "Getting Started," summarizes the information needed to install and configure your ZT 8908.

Chapter 3, "STD 32 Bus Interface," presents a detailed description of the ZT 8908 interface to the STD 32 bus architecture. The topics discussed include compatibility, interrupt structure, and multiple master operation.

Chapter 4, "Interrupt Controller," describes the two Intel-compatible 8259 cascaded interrupt controllers. This chapter summarizes the interrupt sources and the interrupt controllers' register addressing.

Chapter 5, "Counter/Timers," discusses the three programmable counter/timers. It includes a diagram of the counter/timer architecture, and a summary of the operating modes and the programmable registers.

Chapter 6, "DMA Controller," provides an overview of ZT 8908 DMA architecture and briefly describes the DMA controller programmable registers.

Chapter 7, "Real-Time Clock," lists the major features of the real-time clock and briefly describes the real-time clock programmable registers.

Chapter 8, "Serial Controller," discusses operation of the two serial ports and briefly describes the serial controller programmable registers.

Chapter 9, "IEEE Std 1284 Parallel Port Interface," discusses the IEEE Std 1284 compatible printer interface configuration options, address mapping, and interrupt and DMA selection. Programmable registers are also briefly described.

Chapter 10, "Optional IDE Interface," covers the mounting and enabling of an optional local Intelligent Drive Electronics (IDE) interface.

Chapter 11, "System Registers," provides a brief overview of the System registers used to control and monitor a variety of functions on the ZT 8908. System register illustrations are also included.

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Chapter 12, "Watchdog Timer," explains operation of the watchdog timer and includes code for arming and strobing the timer.

Chapter 13, "PCI Mezzanine Local Bus," introduces the features of the Peripheral Component Interconnect (PCI) local bus interface which provides a high speed path between the CPU and peripherals.

Chapter 14, "Programmable LED," provides code for turning the LED on and off.

Chapter 15, "Thermal Considerations," provides operating temperatures and cooling requirements for different processor types.

Chapter 16, "Memory Socket (U14)," explains the functions of memory socket U14, including BIOS recovery and use of video in a STAR SYSTEM.

Appendix A, "Board Configuration," describes BIOS, DIP switch, resistor pack, and cuttable trace configuration on the ZT 8908. This appendix details factory default settings as well as information to tailor your board to a specific application.

Appendix B, "Specifications," contains the electrical, environmental, and mechanical specifications for the ZT 8908. It also provides illustrations and connector pinouts, and tables showing connector pin assignments.

Appendix C, "PCI Configuration Space Map," presents the generic layout of the PCI Configuration Header for all PCI compliant devices. It also contains a table showing the PCI bus mapping of the ZT 8908's on-board devices.

Appendix D, "ZT 8908 Vs. ZT 8905: Technical Differences" describes the technical differences between the ZT 8905 and the ZT 8908 single board computers. It includes information to help existing ZT 8905 customers adapt their applications to the ZT 8908.

Appendix E, "Customer Support," offers technical assistance and warranty information, and the necessary information should you need to return your ZT 8908 for repair.

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1. INTRODUCTION

This chapter provides a brief introduction to the ZT 8908. It includes a product definition, a list of product features, a functional block diagram, and a description of each block. Unpacking information and installation instructions are found in Chapter 2, "Getting Started."

PRODUCT DEFINITION

Electrical, environmental and mechanical specifications of the ZT 8908 are provided in Appendix B, "Specifications".

The ZT 8908 is a highly integrated, enhanced MMX™ single board computer that is factory configured to operate with the Intel Pentium® and AMD-K6™ family of microprocessors. The board meets the needs of a wide range of industrial control and processing applications by operating stand alone, as a single master in an STD 32® architecture, or as a permanent or temporary master in an STD 32 STAR SYSTEM™ architecture. High speed peripheral operation is provided by an on-board PCI expansion interface.

Stand-Alone

The ZT 8908 does not require an STD bus backplane to operate. The ZT 8908 is able to operate stand-alone in many applications because it includes many of the most commonly needed peripheral devices. On-board peripheral devices include:

- 2 or 4 Mbyte flash file system for disk support
- PCI local bus expansion port
- Optional IDE hard disk interface
- Keyboard controller
- Serial I/O
- Printer interface
- Speaker interface
- Interrupt controllers
- Counter/timers
- Watchdog timer
- Real-time clock

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STD 32 Single Master Architecture

The ZT 8908 supports additional memory and I/O through the STD 32 bus. Both Standard Architecture (8- and 16-bit) and Extended Architecture (8-, 16-, and 32-bit) transfer types are dynamically supported through the STD 32 interface. Jumperless configuration of interrupt, DMA, and STD 32 bus memory and I/O space is performed through the BIOS Setup utility.

STD 32 Multiple Master Architecture

The ZT 8908 can be configured to operate in a multiple master architecture as either a permanent master or a temporary master. With this architecture, up to seven ZT 8908 boards share STD bus memory and I/O resources. The permanent master provides system clock and reset functions as well as the pull-up signals for the open-collector signals on the STD 32 bus. The permanent master is also responsible for initializing shared memory and other system I/O on behalf of any temporary masters. The STAR BIOS manages all of the system initialization.

FEATURES

- STD 32 bus compatible
- PCI compatible local bus
- Single and multiple master operation
- Pentium processor up to 233 MHz and AMD-K6 processor up to 266 MHz
- Numeric coprocessor support (Pentium)
- L1 cache depending on CPU
- 512 Kbytes of L2 cache
- Optional IDE hard disk interface (local to ZT 8908)
- 32, 64, or 128 Mbytes of DRAM memory
- 2 Mbytes of flash memory (expandable to 4 Mbytes)
- Optional 32-bit PCI local bus peripheral support (through the PCI mezzanine connector)

  – Super VGA (640 x 480 x 16 Mbytes through 1280 x1024 x 64 Kbytes)

  – Contact Ziatech for additional peripherals

- Standard AT® peripherals include:

  – Two enhanced interrupt controllers (8259)

  – Three counter/timers (one 8254)

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  – Real-time clock/CMOS RAM (146818)
  – Two enhanced DMA controllers (8237)
  – 8042 compatible keyboard controller
- IEEE Std 1284 printer port (ECP/EPP compatible)
- Two 16C550 RS-232 serial ports
- PS/2 Mouse interface
- Keyboard interface
- USB Type A interface (requires third party software)
- Speaker interface
- Two on-board high efficiency 3.3 V DC-DC converter
- Push-button reset
- Software programmable LED
- DC power monitors (3.3 V and 5 V)
- Compatible with the following software: MS-DOS®, OS/2®, QNX®, UNIX®, VRTX32®, VxWorks®, Windows 3.1® and 3.11, Windows 95, and Windows NT®
- DOS and STAR BIOS options
- STD 32 bus standard 4.5" x 6.5" board format
- Five-year warranty

DEVELOPMENT CONSIDERATIONS

Ziatech offers DOS and STD 32 STAR SYSTEM™ software development systems for ZT 8908 applications. Ziatech DOS is Microsoft's MS-DOS residing on the ZT 8908. The DOS system provides a development platform similar to a PC, enabling applications to be developed quickly. DOS includes support for many of the ZT 8908 peripherals and is supported by a large number of development tools such as program editors, compilers, assemblers, and debuggers. Refer to the Ziatech system manual for configuration and operating instructions.

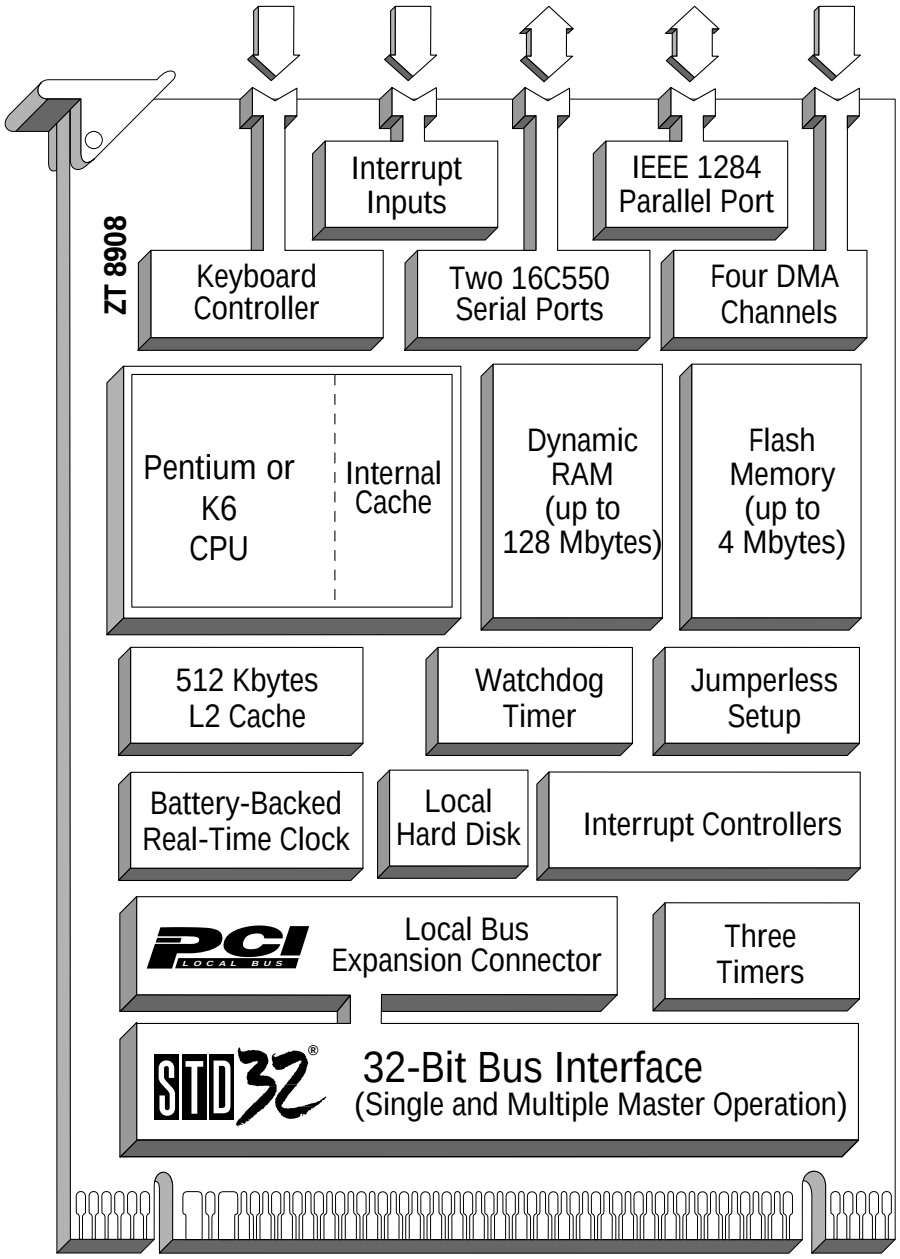
The STD 32 STAR SYSTEM is the DOS platform operating on more than one master in a single STD bus system. Each master includes local memory, local I/O, and the DOS operating system. Each master is capable of sharing STD bus memory and I/O, such as fixed disks, floppy disks, and video. Refer to the STAR SYSTEM operating manual for configuration and operating instructions.

Ziatech also offers software development kits for QNX® and VxWorks® operating systems. Contact Ziatech for details.

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FUNCTIONAL BLOCKS

The "Functional Block Diagram" illustrates the ZT 8908's major functional blocks. The blocks correspond to topics remaining in this chapter.



Functional Block Diagram

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STD Bus Interface

The ZT 8908 operates in the STD 32 system. In an STD 32 system, data transfers are dynamically sized for either 8- or 16-bit Standard Architecture or 8-, 16-, or 32-bit Extended Architecture transfers. All STD-80 compatible memory and I/O boards are supported using 8-bit Standard Architecture transfers. STD 32 compatible memory and I/O boards are dynamically sensed to determine the width of the data transfer.

The STD 32 system provides the platform needed for multiple master operation. In a multiple master system, up to seven processor boards share STD bus resources with a fixed or rotating priority granted by an external bus arbiter, such as the ZT 89CT39. See Chapter 3, "STD 32 Bus Interface," for a detailed description of the ZT 8908 interface to the STD 32 bus architecture.

Pentium and AMD-K6 Processors

The ZT 8908 supports Pentium® processors and AMD-K6™ MMX™ Enhanced processors. The ZT 8908 operates the external microprocessor bus at either 50, 60, or 66 MHz. Pentium processors and AMD-K6 processors operate internally at 1.5x, 2x, 2.5x, 3x, 3.5x, and 4.5x the microprocessor bus, supporting processor operation up to 300 MHz.

The PCI bus always operates at 1/2 the external microprocessor bus speed. Not all processor speeds are offered by Ziatech. Contact Ziatech for latest product offerings.

Pentium processors and AMD-K6 processors include a minimum of 16 Kbytes of cache (referred to as L1 cache). This L1 cache supports both write-through and write-back cache. A secondary 512 Kbytes of L2 cache is standard on the ZT 8908.

Intel 430TX PCIset Interface Chip

The Intel 430TX PCIset is designed to maximize throughput on the PCI bus. It is a third generation PCI chipset capable of burst mode transfers to 110 Mbytes per second. The 430TX PCIset sets the standard for the Pentium processor-class of computers.

Refer to Appendix C, "PCI Configuration Space Map," for more information about the Intel 430TX PCIset.

3.3 Volt And Split Voltage Technology

The ZT 8908 contains dual DC/DC converters to support Intel processors that use STD (standard voltage), VRE (reduced and shifted voltage), or a split voltage (P55C MMX processor). One converter is used for the processor's VI/O and other 3.3 V devices (such as DRAM or chipset). The other converter is used to drive the processor core for split voltage processors. The board is configured from the factory to the correct voltage for the loaded processor.

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Memory and I/O Addressing

The ZT 8908 includes two 72-pin SO-DIMM sockets that support up to 128 Mbytes of DRAM. The ZT 8908 also supports flash memory soldered directly on the board. Memory operations not decoded for on-board DRAM are forwarded to the STD 32 bus. EA memory interfaces (for example, ZT 8920) may be mapped anywhere above local memory space in the 32-bit EA address space. SA peripherals are limited to the lower 16 Mbyte address space because the SA memory address range is only 24 bits deep. If 32 Mbytes or more of local DRAM are loaded on the ZT 8908, SA peripherals must be located in the lower 1 Mbyte address space. STD 32 memory addressing is configured through the BIOS Setup utility.

The ZT 8908 also provides 512 Kbytes of L2 cache to enhance CPU performance. The DRAM's most recently used data is stored in and retrieved from cache, considerably reducing the need to access the DRAM. Note that the ZT 8908 only caches the first 64 Mbytes of DRAM.

For more information, see the topics "Memory Configuration" and "Setup" in Chapter 2.

The ZT 8908 also includes many I/O peripherals required for industrial control applications. 8- and 16- bit SA I/O peripherals and 8-, 16-, and 32-bit EA I/O peripherals are supported. For both SA and EA I/O, addressing is limited to 64 Kbytes (16 bits). The STD bus I/O expansion signal, IOEXP, is dynamically driven low in the FC00h-FFFFh address range to prevent older STD I/O boards that decode less than 16 bits of address from being redundantly mapped.

For more information, see "I/O Configuration" in Chapter 2.

PCI Local Bus

The ZT 8908 supports high speed peripheral interfacing through the PCI Mezzanine Local Bus Interface Connector (J5). Only one mezzanine adapter board at a time may be connected to J5. The mezzanine connector supports 32-bit data transfers. A mezzanine board/ZT 8908 combination occupies just one slot in an STD 32 card cage.[†]

The ZT 8908 also provides a pass-down connector (J10) for video signals from VGA mezzanine boards such as the zPM11 Super VGA PCI Mezzanine Adapter. The video signals are then routed to the multi-I/O connector (J4) for display interfacing. See Chapter 13, "PCI Mezzanine Local Bus" for more details on the PCI interface.

[†] A ZT 8908 with the fan/heatsink option requires two slots.

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Serial I/O

The ZT 8908 includes two 16C550 PC-compatible serial ports. The serial ports are implemented with a 5 V charge pump technology. Both serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115.2 Kbaud.

The serial ports are configured as DTE and are available through the multi-I/O connector (J4). The ZT 90243 Multi-I/O cable converts the multi-I/O interface to a standard 9-pin D-shell male connector. A null-modem option is available to convert the DTE configuration to DCE. Adapter board options are also available to convert the RS-232 interface to an RS-485 interface.

See Chapter 8, "Serial Controller," for information about the ZT 8908's serial controller.

Interrupts

The ZT 8908's two enhanced 8259 style interrupt controllers provide a total of 15 interrupt inputs. Interrupt controller features include support for level-triggered and edge-triggered inputs, fixed and rotating priorities, and individual input masking. Interrupt sources include counter/timers, serial I/O, real-time clock, keyboard, printer, and multiple master communications.

The ZT 8908 includes five frontplane and five backplane interrupt sources. Enhanced capabilities include the ability to configure each interrupt level for active high going edge or active low level inputs.

All interrupt routing for STD 32 and frontplane interrupt sources is done through the BIOS Setup utility, allowing jumperless configuration. The PCI enumerator can also configure up to four PCI interrupts.

See Chapter 4, "Interrupt Controller," for more information.

Counter/Timers

Three 8254 style counter/timers are included on the ZT 8908 as defined for the AT. Operating modes supported by the counter/timers include interrupt on count, frequency divider, square wave generator, software triggered, hardware triggered, and one shot.

See Chapter 5, "Counter/Timers," for more information.

DMA

The ZT 8908's two enhanced 8237 style DMA controllers provide a total of one STD 32 and three frontplane DMA channels for data transfers between system I/O and local memory. The DMA channels support STD 32 bus DMA slaves by managing the data

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transfers between the slaves and local memory. Additional features of the DMA channels include auto initialization, address increment or decrement, and software DMA requests. Enhanced DMA capabilities include support for higher speed (8 Mbyte/sec) transfer types and 32-bit memory addressing.

One DMA channel is available through the STD bus BUSRQ and BUSAK* signals. This is configurable as either an 8-bit DMA channel (DRQ2) used primarily for floppy disk operation or a 16-bit DMA channel (DRQ5). Three additional DMA channels are available through the frontplane DMA connector (J7).

See Chapter 6, "DMA Controller," for more information.

Watchdog Timer

The watchdog timer optionally monitors system operation. Failure to strobe the watchdog timer within a set time period results in a system reset.

See Chapter 12, "Watchdog Timer," for more information.

Real-Time Clock

The real-time clock performs timekeeping functions and includes 256 bytes of general-purpose battery-backed CMOS RAM. Timekeeping features include an alarm function, a maskable periodic interrupt, and a 100-year calendar. The system BIOS uses a portion of this RAM for BIOS Setup information. The system BIOS is also Year 2000 compliant.

See Chapter 7, "Real-Time Clock," for more information.

Keyboard Controller

The ZT 8908 includes a PC/AT® keyboard controller. Off-board keyboard controllers are not supported by the ZT 8908. Keyboard connection is available through the multi-I/O connector (J4).

PS/2 Mouse Controller

The ZT 8908 includes a PS/2 mouse controller to support either a mouse or keyboard. Mouse connection is available through the multi-I/O connector (J4).

Universal Serial Bus (USB)

The emerging Universal Serial Bus (USB) will provide a common interface to slower speed peripherals. Functions such as keyboard, serial ports, printer port, and mouse ports will be consolidated into USB, greatly simplifying future cabling requirements. The ZT 8908 provides one USB port through the multi-I/O connector (J4).

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Note: The Ziatech BIOS does not directly support USB. This feature requires third party software.

IEEE Std 1284 Parallel Port/Printer Interface

The ZT 8908 includes an IEEE® Std 1284 compatible parallel port for connection to a printer or other parallel port devices such as software keys required by many application packages. The parallel port is ECP/EPP compatible.

The printer interface is available through the multi-I/O connector (J4). An optional transition cable (ZT 90243) provides a 25-pin D-shell connector for software key or printer support. The mode (Normal, Extended, EPP, ECP) for the printer interface is selectable through the BIOS Setup utility.

See Chapter 9, "IEEE Std 1284 Parallel Port Interface," for more information.

Speaker Interface

The ZT 8908 supports an external AT-compatible speaker through connector J3.

Optional IDE Interface

The ZT 8908 can be ordered (Option D1) with an on-board IDE interface connector (J8) for an IDE hard drive. This option is useful for single board operation (without the STD 32 backplane) or for STAR SYSTEM operation where it is desirable to have a local boot device that is independent of other STAR SYSTEM CPUs. This option includes a 2.5" IDE interface mounted directly to the solder side of the ZT 8908. When used in the STD 32 chassis, the IDE drive occupies one slot more than the standard ZT 8908.

See Chapter 10, "Optional IDE Interface," for more information.

The ZT 8908 supports a local Intelligent Drive Electronics (IDE) hard disk through an optional IDE interface connector (J8). The hard drive mounts to the bottom side of the ZT 8908 either directly or on an adapter board and is attached with three screws. This feature is useful for single board applications as well as STAR SYSTEMs where the ZT 8908 needs to have a local (non-shared) hard disk.

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2. GETTING STARTED

This chapter summarizes the information needed to make the ZT 8908 operational. Read this chapter before attempting to use the board.

UNPACKING

Please check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Ziatech for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Save the anti-static bag for storing or returning the ZT 8908.

Do not return any product to Ziatech without a Return Material Authorization (RMA) number. Appendix E, "Customer Support" explains the procedure for obtaining an RMA number from Ziatech.



Warning: Like all equipment utilizing MOS devices, the ZT 8908 must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the ZT 8908 to handle the boards.

SYSTEM REQUIREMENTS

The ZT 8908 is designed for use with or without an STD 32 bus backplane. The ZT 8908 is electrically, mechanically, and functionally compatible with the *STD 32 Bus Specification and Designer's Guide* (ZT MSTD32) for STD bus applications.

The ZT 8908 requires both 5 V and 12 V power for proper operation.

Ziatech recommends vertical mounting. The ZT 8908 can operate from 0º C to 70º C depending on the CPU and the fan/heatsink installed on the board. Refer to Appendix B, "Specifications," for operating temperatures with different CPU options.

MEMORY CONFIGURATION

The ZT 8908 addresses up to 4 Gbytes of memory. The address space is divided between memory local to the board, memory located on the PCI expansion interface, and memory on the STD bus. Any memory not reserved or occupied by a local memory device (DRAM/flash) or the STD bus is available for PCI bus expansion. The memory address regions available for the STD bus are configured through the BIOS Setup mechanism. During local memory operations, the STD bus is held static to decrease system electrical noise and power consumption.

STD bus memory is supported through either Standard Architecture (SA8 or SA16) transfers, or Extended Architecture (EA8, EA16, or EA32) transfers. The ZT 8908

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supports the STD bus wait request signal, WAITRQ*, to interface to SA memory boards with longer access time requirements than those defined by the STD-80 and STD 32 specifications. The signal EXRDY is supported for EA peripherals that require additional transfer time.

The ZT 8908 is populated with several memory devices. Local DRAM implements two 72-pin SO-DIMM modules for up to 128 Mbytes of DRAM (32 Mbytes minimum). Memory modules must be added in pairs due to the 64-bit memory architecture of the AMD-K6 and Pentium processors.

The ZT 8908 also provides 512 Kbytes of L2 cache to enhance CPU performance. The DRAM's most recently used data is stored in and retrieved from cache, considerably reducing the need to access the DRAM. Note that the ZT 8908 only caches the first 64 Mbytes of DRAM.

Local flash memory is soldered directly to the board. Up to two 2 Mbyte Intel flash devices may be factory installed.

The "Memory Address Map" shows default memory addressing for the ZT 8908.

I/O CONFIGURATION

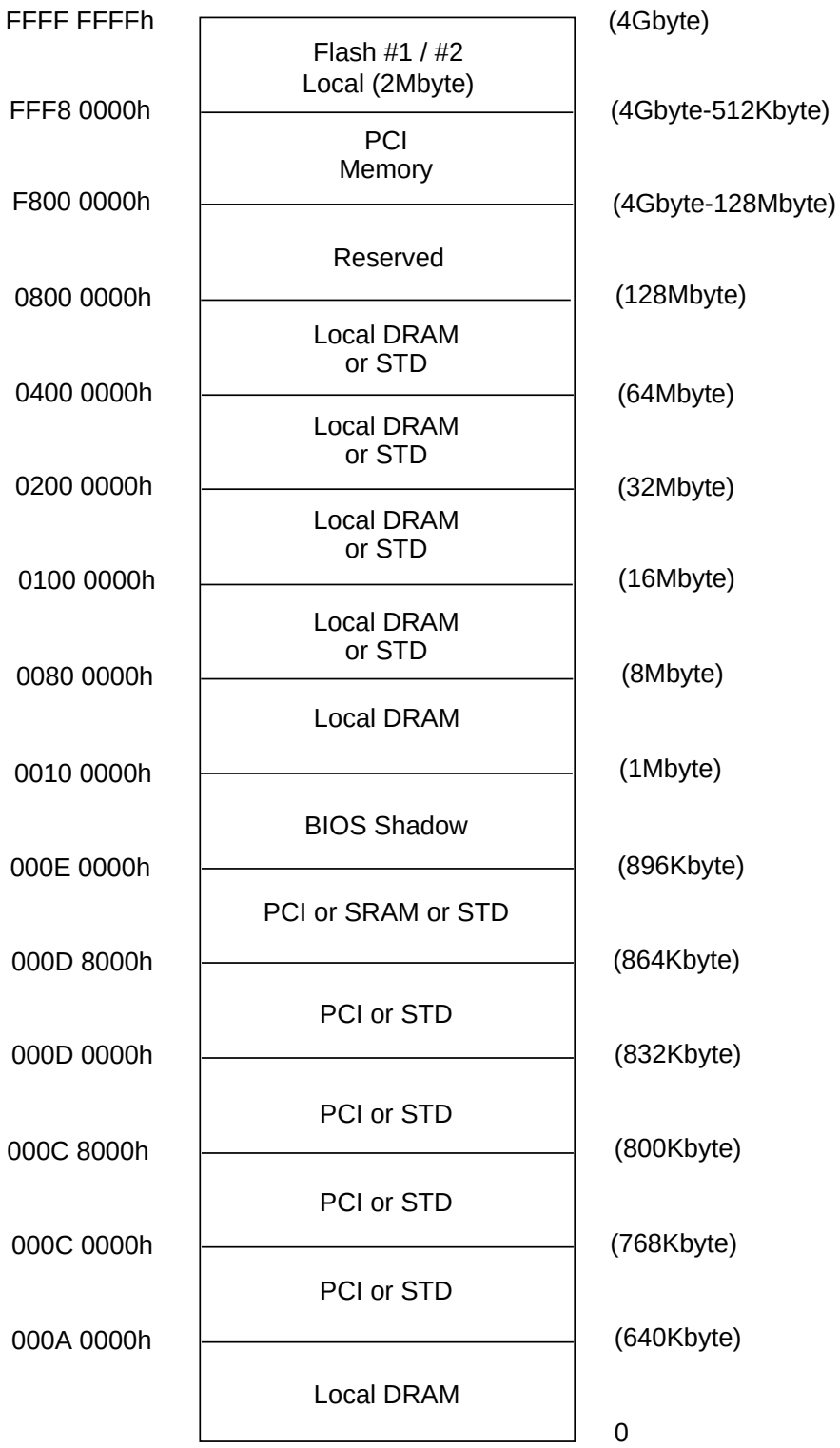
The ZT 8908 addresses up to 64 Kbytes of I/O using a 16-bit I/O address. The address space is divided between I/O local to the board and I/O on the STD bus. Any I/O space not occupied by a local I/O device or STD bus is available for PCI bus expansion. The I/O address regions available for the STD bus are configured through the BIOS Setup utility (discussed in the section "Setup" later in this chapter). During local I/O operations, the STD bus is held static to decrease system electrical noise and power consumption.

STD bus I/O is supported through either Standard Architecture (SA8 or SA16) transfers, or Extended Architecture (EA8, EA16, or EA32) transfers. The ZT 8908 supports the STD bus wait request signal, WAITRQ*, to interface to I/O boards with longer access time requirements than those defined by the STD-80 and STD 32 specifications. The signal EXRDY is supported for EA peripherals that require additional transfer time.

The STD bus I/O expansion signal, IOEXP, is also supported. The IOEXP signal is automatically driven low over the I/O address range FC00h to FFFFh. Application software should use this address range to access STD bus I/O boards decoding IOEXP and fewer than 16 bits of address to prevent the board from being redundantly mapped throughout the 64 Kbyte I/O address space.

The ZT 8908 is populated with many of the most commonly used I/O peripheral devices for industrial control and computing applications. The I/O address location for each of the peripherals is shown in the "I/O Address Range Selection" table.

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Memory Address Map

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I/O Address Range Selection

I/O Address Range	I/O Usage (see note)	Function
8000h - FFFFh	STD 32 Address Space	
5000h - 7FFFh	PCI I/O Address Space	
4E70h - 4FFFh	PCI I/O Address Space	
46E8h - 46EFh	STD 32 or PCI I/O Address Space	VGA Configuration Register
4000h - 46E7h	PCI I/O Address Space	
1000h - 3FFFh	PCI I/O Address Space	
0C00h - 0FFFh	PCI I/O Address Space	
0900h - 0BFFh	STD 32 Address Space	
0800h - 08FFh	PCI I/O Address Space	
0780h - 07FFh	STD 32 Address Space	
0700h - 077Fh	STD 32 or PCI I/O Address Space	LPT ECP Ports Bits
0500h - 06FFh	STD 32 Address Space	
0400h - 04FFh	PCI I/O Address Space	
03F8h - 03FFh	STD 32 or PCI I/O Space	COM1 Register Set
03F6h	STD 32 or PCI I/O Space	Primary IDE Registers Set
03F0h - 03F5h, 03F7h	STD 32 or PCI I/O Space	Floppy Register Set
03E0h - 03EFh	STD 32 Address Space	
03B0h - 03DFh	STD 32 or PCI I/O Address Space	VGA Register Set
0380h - 03AFh	STD 32 Address Space	
037Ch - 037Fh	STD 32 or PCI I/O Address Space	LPT EPP
0378h - 037Bh	STD 32 or PCI I/O Address Space	LPT Port
0376h	PCI I/O Address Space	Secondary IDE Register
0370h - 0375h, 0377h	STD 32 Address Space	
0300h - 036Fh	STD 32 Address Space	
02F8h - 02FFh	STD 32 or PCI I/O Address Space	COM2 Register Set
0200h - 02F7h	STD 32 Address Space	
01F8h - 01FFh	STD 32 Address Space	
01F0h - 01F7h	STD 32 or PCI I/O Address Space	Primary IDE Register Set

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I/O Address Range Selection (con'd)

I/O Address Range	I/O Usage (see note)	Function
0178h - 01EFh	STD 32 Address Space	
0170h - 0177h	PCI I/O Address Space	Secondary IDE Register Set
0100h - 016Fh	STD 32 Address Space	
00F0h - 00FFh	PCI I/O Address Space	Onboard Coprocessor
00E0h - 00EFh	PCI I/O Address Space	Reserved
00C0h - 00DFh	PCI I/O Address Space	Onboard Slave DMAC
00B0h - 00BFh	PCI I/O Address Space	Reserved
00A0h - 00AFh	PCI I/O Address Space	Onboard Interrupt Controller
0093h - 009Fh	PCI I/O Address Space	Reserved
0092h	PCI I/O Address Space	Fast Reset & Gate A20
0090h - 0091h	PCI I/O Address Space	Reserved
0081h - 008Fh	PCI I/O Address Space	Onboard DMA Page Registers
0080h	PCI I/O Address Space	Diagnostic Port 080h
007Bh - 007Fh	PCI I/O Address Space	Reserved
0078h - 007Ah	PCI I/O Address Space	ZT 8908 System Register 0 - 2
0070h - 0077h	PCI I/O Address Space	Onboard Real time Clock
0068h - 006Fh	PCI I/O Address Space	
0067h	STD 32 or PCI I/O Address Space	VGA Control Register
0065h – 0066h	PCI I/O Address Space	
0064h	STD 32 or PCI I/O Address Space	Keyboard
0061h - 0063h	PCI I/O Address Space	
0060h	STD 32 or PCI I/O Address Space	Keyboard
0050h - 005Fh	PCI I/O Address Space	Reserved
0040h - 004Fh	PCI I/O Address Space	Onboard Counter Timers
0030h - 003Fh	PCI I/O Address Space	Reserved
0020h - 002Fh	PCI I/O Address Space	Onboard master Interrupt
0000h - 001Fh	PCI I/O Address Space	Onboard Master DMAC

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Notes:

1. STD 32 Address Space refers to STD 32 backplane devices.
2. PCI I/O Address Space refers to mezzanine devices or devices onboard the ZT 8908.

INTERRUPTS

The ZT 8908 includes two Intel-compatible 8259 cascaded interrupt controllers that provide a programmable interface between interrupt-generating peripherals and the CPU. The interrupt controllers monitor 15 interrupts with programmable priority. When peripherals request service, the interrupt controller interrupts the CPU with a pointer to a service routine for the highest priority device.

The interrupt architecture is presented in the "Interrupt Architecture" table. Interrupt configuration is performed through Screen 2 of the BIOS Setup utility, allowing the user to set up the interrupt architecture to the needs of the application. The Setup utility allows most of the interrupt controller interrupts to be configured from a variety of interrupt sources. See "Setup" for more information. The ZT 8908 supports the Extended Mode register, which allows individual programming of low-level triggered or active high-edge triggered interrupts.

Note: The message "Warning: No PCI Interrupts Available" may appear at boot time. This is because the default configuration allocates no interrupts as PCI interrupts. You may ignore this message if you are not using USB devices and if no interrupts are needed for the optional PCI mezzanine device. PCI interrupts may be allocated through the BIOS Setup utility. Any of the interrupts IR10-IR12 can be set to PCI. See the "Setup" topic for more information.

For more information on the interrupt controllers, see Chapter 4, "Interrupt Controller."

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Interrupt Architecture

Notes	CPU Interrupt	Programmable Interrupt Sources (default in bold)
1	IRQ0	**System Timer 0**
2	IRQ1	**Local keyboard** or **INTRQ1***
3	IRQ2	**Cascade**
2	IRQ3	**COM2**
2	IRQ4	**COM1**
2	IRQ5	**INTRQ4***
2	IRQ6	**INTRQ2***
2	IRQ7	**Local LPT**
4	IRQ8	**Real-Time Clock**
2	IRQ9	**INTRQ***
2	IRQ10	**J6, pin 4** or PCI
2	IRQ11	**J6, pin 6** or PCI
2	IRQ12	**J6, pin 10** or PCI
5	IRQ13	**Math Coprocessor**
2, 6	IRQ14	**INTRQ3*** or Local IDE
7	IRQ15	**J6, pin 8** or INTS

Notes:

1. CTC1-Ch0: System Timer.
2. Also supports INTRQ*, INTRQ1* INTRQ2*, INTRQ3*, INTRQ4*, and J6--pins 2, 4, 6, 8, 10.
3. Second interrupt controller (8259).
4. Real Time Clock interrupt.
5. Math coprocessor exception interrupt.
6. Enable the ZT 8908 for either local IDE or STD 32 IDE operation through the BIOS Setup utility. See "Selecting IDE Operation Type" in Chapter 10 for details.
7. The default IRQ15 source depends on the status of cuttable trace CT45 (see Appendix A). Other interrupt sources are possible for IRQ15 with custom software configuration. Contact Ziatech.

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CONNECTORS

As shown in the "Connector Locations" figure, the ZT 8908 includes several connectors to interface to application-specific devices. A brief description of each connector is given in the "Connector Assignments" table. Refer to the "Connectors" section in Appendix B for complete connector descriptions and connector pinouts, as well as cabling information.

DIP SWITCH AND CUTTABLE TRACE DESCRIPTIONS

The ZT 8908 includes several DIP switch and cuttable trace configuration options for features that cannot be provided for through the Setup utility. Refer to Appendix A, "Board Configuration," for details.

REMOVING THE ZPM MEZZANINE CARD

Ziatech zPM mezzanine cards plug into the 150-pin PCI mezzanine connector provided on many Ziatech CPUs (J5 on the ZT 8908). Mechanical connection of the boards is reinforced by metal or nylon standoffs that are screwed through mounting holes in each board.



Caution: If it is necessary to disconnect a zPM mezzanine card, Ziatech recommends removing only the screws attaching the card to the standoffs. If it is necessary to remove the standoffs from the CPU, be aware that on some CPUs washers may be located between the PCB and the standoffs. Be sure to retain and reinstall these washers to their original position if they are removed for any reason.

Also take care when installing and removing the zPM mezzanine card to prevent premature wear or accidental bending of the 150-pin (and on some mezzanine cards, an additional 16-pin) connector. When removing the card, disengage the pins evenly across the length of the connectors instead of prying only from one side. It may be helpful to gently wiggle the card from side to side when removing it.



Warning: To avoid damage to the CPU and the mezzanine card, install and remove the mezzanine card at a static-free workstation.

SETUP

The ZT 8908 has many features that can be configured with the BIOS Setup utility. The Setup utility is executed during the boot sequence when the **"s"** key is typed. In DOS systems, Setup may be executed by running the SETUP.COM program from the command line.

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The BIOS Setup utility on all Ziatech CPUs allows configuration of options such as base memory and extended memory size selection, boot source, hard disk type, and floppy disk type. On the ZT 8908, the BIOS Setup also allows routing of interrupts, memory mapping, and I/O mapping for the STD 32 bus. Previous generation CPU products required jumpers to configure these options. This change makes configuration both faster and more intuitive. PCI peripherals are also automatically configured through the BIOS.

For setup options specific to the ZT 8908, refer to the topic, "ZT 8908-Specific Setup Options," in Appendix A.

BIOS SETUP Screens

The BIOS Setup utility for the ZT 8908 is organized as two screens, listed below.[†]

- **Screen 1: Generic options list.** Screen 1 lists the options shared among all Ziatech CPUs. Base memory and extended memory size selection, boot source, hard disk type, and floppy disk type are configurable through this screen.
- **Screen 2: ZT 8908-specific Setup options.** Options such as interrupt routing and STD 32 memory addressing are configurable through this screen. Screen 2 is detailed in the section "ZT 8908-Specific Setup Options" in Appendix A.

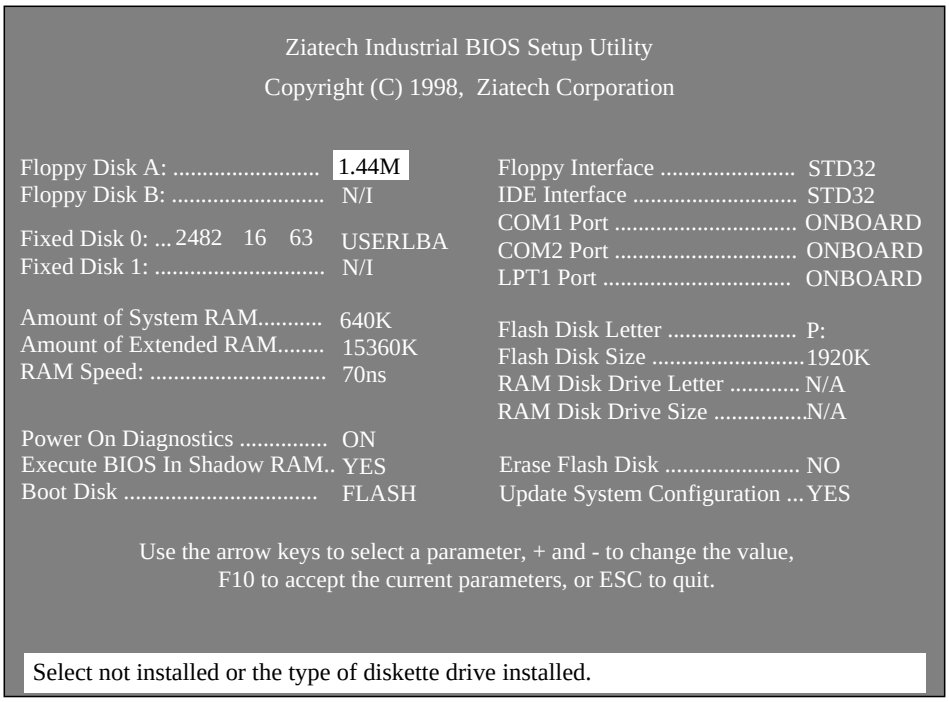
The parameters in the Setup screens are easily changed. Use the arrow keys to select a parameter, then press **+** or **-** to step through the valid choices for that parameter. A dynamic help line at the bottom of the screens helps you determine how to set each parameter. SETUP accepts only valid parameter sets: if changing one parameter invalidates another, SETUP automatically updates the invalid parameter. After setting the parameters, press the F10 key to accept them. Press the **Page Down** and **Page Up** keys to switch between Setup screens.

System Configuration Overview

The Ziatech Industrial BIOS and MS-DOS operating system software is preprogrammed in the ZT 8908's onboard flash memory. The BIOS includes embedded support to allow the ZT 8908 flash memory to be used as a solid-state drive (SSD) in the MS-DOS environment. Ziatech also provides SSD support for other popular operating systems such as Windows NT and QNX (contact Ziatech for SSD drivers for specific operating systems).

[†] A third screen for STAR SYSTEM configuration options is available when running SETUP on permanent master CPUs. Refer to the *STD 32 STAR SYSTEM User's Manual* for more information.

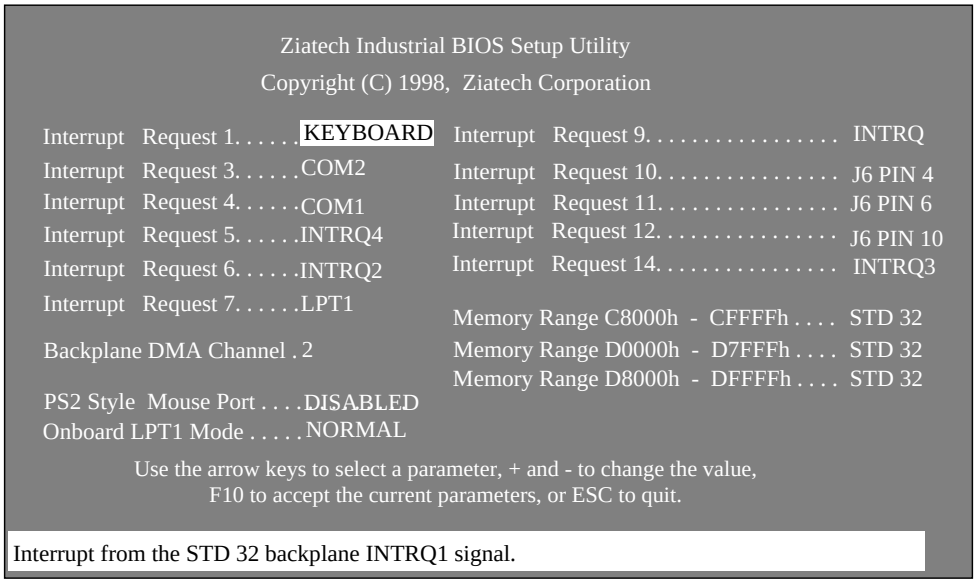
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ZT8908

BIOS Setup Utility: Screen 1

Generic Setup Options



ZT8908

BIOS Setup Utility: Screen 2

ZT 8908-Specific Setup Options

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Operating System Installation

It may be necessary to install an operating system such as Windows NT or QNX on the ZT 8908. This section describes the generic OS installation process. For OS-specific information, refer to the documentation provided by the OS vendor.

Note: if the installation requires a CD-ROM drive, the appropriate drivers must first be installed in order to access the CD-ROM drive.

1. Use Screen 1 in the BIOS Setup utility to configure the appropriate peripheral devices. Note that the Fixed Disk parameters (used for EIDE drives) include an "AUTO" setting which will cause SETUP to query the drive to determine the correct geometry (cylinders/heads/sectors).

2. Select the proper boot source in the Setup utility depending on the OS installation media that will be used. For example, if the OS includes a bootable installation floppy, select "FLOPPY" for "Boot Disk" and reboot the system with the installation floppy installed in the floppy drive.

3. Proceed with the OS installation as directed, being sure to select appropriate device types if prompted. See the "Onboard Device PCI Bus Mapping" table in Appendix C for a list of the PCI devices used on the ZT 8908.

4. When installation is complete, reboot the system and set the SETUP "Boot Disk" parameter for the appropriate boot media.

Warnings

The message "Warning: No PCI Interrupts Available" may appear at boot time. This is because no interrupts have been allocated as PCI interrupts. You may ignore this message if you are not using USB devices and if no interrupts are needed for the optional PCI mezzanine device. PCI interrupts may be allocated through the BIOS Setup utility. Any of the interrupts IR10-IR12 can be set to PCI. See the Setup topic for more information.

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3. STD 32 BUS INTERFACE

The ZT 8908 includes several I/O devices common to industrial control applications. The ZT 8908 also operates with the STD 32 bus architecture to support additional I/O and memory mapped devices as required by the application. This chapter discusses the STD 32 architecture and its effect on the operation of the ZT 8908.

STD 32 BACKGROUND

The *STD-80 Series Bus Specification*, developed in the early 1980s by Ziatech Corporation, defines the electrical, mechanical, and functional characteristics of an STD bus system based on the 8088 series of microprocessors. Features of an STD-80 system include an 8-bit data bus, 24-bit address bus, and single bus master operation.

In the late 1980s, Ziatech developed the *STD 32 Bus Specification and Designer's Guide* as an extension to the *STD-80 Series Bus Specification*. Features of an STD 32 system include compatibility with STD-80 memory and I/O boards, expansion capabilities of up to a 32-bit data bus and a 32-bit address bus, and support for multiple bus master operation.

STD-80 PERIPHERAL SUPPORT

The ZT 8908 is electrically compatible with Revision 2.3 of the *STD-80 Series Bus Specification* (Ziatech part number ZT MSTD80), allowing peripherals that were designed for that specification to be used with the ZT 8908 in an STD 32 backplane. The ZT 8908 cannot be used in an STD-80 backplane because of the additional signals needed for EA 32-bit addressing. However, STD-80 boards can be used with the ZT 8908 in an STD 32 backplane. STD-80 superset features supported by the ZT 8908 include:

- A 24-bit address bus
- Four additional maskable interrupts
- Dynamically driven I/O expansion
- DMA slave support

The following topics discuss these features.

Address Multiplexing

The *STD-80 Series Bus Specification* defines a multiplexing scheme to transfer address lines A16 through A19 across the lower half of the data bus during the start of each

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memory cycle. The ZT 8908 extends this concept by also transferring address lines A20 through A23 across the upper half of the data bus.

This feature is especially useful if all memory mapped STD bus boards used in the system decode 24 bits of address. If a memory mapped board decodes fewer than 24 bits, the board appears multiple times in the 24-bit memory map.

Interrupts

The *STD-80 Series Bus Specification* defines a single interrupt signal, INTRQ* (P44). If STD bus maskable interrupts are used in the application, the ZT 8908 is configurable to receive INTRQ* and four optional interrupts: INTRQ1* (P37), INTRQ2* (P50), INTRQ3* (E67), and INTRQ4* (P6). STD bus peripheral boards must be capable of generating an interrupt on INTRQ1*, INTRQ2*, INTRQ3*, and INTRQ4* to use this feature.

I/O Expansion

The *STD-80 Series Bus Specification* defines an I/O expansion signal, IOEXP, used to reduce addressing redundancy of an I/O board decoding fewer than 16 address lines. The ZT 8908 automatically drives this signal low when the application software performs an I/O read or write to I/O address locations in the range FC00h through FFFFh. To use this feature:

- The I/O mapped STD bus board is configured to respond to an active low IOEXP.
- The application software assigns the board to address FC00h plus the board configuration offset.

DMA Slave Support

The ZT 8908 supports DMA slaves through either backplane or frontplane signaling. The STD 32 specification defines control signals for backplane DMA transfers to peripherals such as the ZT 8954 Floppy Disk Interface. The ZT 8908 supports up to three frontplane DMA slaves controlled through connector (J7).

STD 32 BUS COMPATIBILITY

The ZT 8908 is compatible with the *STD 32 Bus Specification and Designer's Guide* (Ziatech part number ZT MSTD32). The STD 32 bus allows both older STD-80 style peripherals and new higher performance peripherals as defined by STD 32 to be used in the same backplane.

STD 32 separates older peripherals and newer peripherals into Standard Architecture, Extended Architecture, and Multiprocessing, as described in the following topics.

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Standard Architecture

Standard Architecture 8- and 16-bit peripherals are referred to as SA8 and SA16, respectively. The ZT 8908 supports interfacing to both SA8 and SA16 peripherals. Older STD-80 style peripherals are compatible with SA8 transfers, allowing the ZT 8908 to support these peripherals. The ZT 8908 automatically determines the type of transfer at the start of each STD bus operation. If the application software includes a 16-bit operation with an 8-bit STD bus (SA8) board, the ZT 8908 automatically reduces the transfer into two STD bus cycles. If the application software includes a 16-bit operation with a 16-bit STD 32 (SA16) board, the ZT 8908 performs the transfer in a single STD bus cycle. A single STD cycle for SA peripherals is typically seven STD 32 clock periods.

Extended Architecture

Extended Architecture 8-, 16-, and 32-bit peripherals are referred to as EA8, EA16, and EA32, respectively. The ZT 8908 supports interfacing to all three data width types. The ZT 8908 dynamically senses the type of peripheral at the start of the backplane cycle and will scale the transfer to match the data width of the peripheral. The memory addressing for EA peripherals is 32 bits (4 Gbytes); I/O addressing is 16 bits (64 Kbytes). EA cycles are typically completed in three STD 32 clock periods.

Multiprocessing

In addition to the different data transfer modes, the STD 32 system has another advantage: it supports up to seven processor boards in a single system. With the addition of an STD bus arbiter, such as the ZT 89CT39, multiple ZT 8908 boards have fixed or rotating priority access to STD bus memory and I/O resources. This architecture is useful for applications that can be divided into modular control blocks, with each module running on a unique ZT 8908. Ziatech manufactures several boards that are compatible with the multiprocessing architecture.

STD 32 Compliance Levels

STD 32 features are discussed in terms of compliance levels. The compliance codes can be used to determine the general capabilities of a board, particularly when configuring a system composed of boards from different manufacturers.

Permanent Master:	EA32, EA16, EA8, SA16, SA8-{MD}, I, SDMA8, SDMA16, SDMABP
Temporary Master:	SA16, SA8-{MX}, I, SDMA8, SDMA16, SDMABP

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The following are brief descriptions of the STD 32 compliance levels supported by the ZT 8908.

EA8, EA16, EA32 — Supports 8-bit, 16- and 32-bit data transfers with STD 32 Extended Architecture signal format and timings. The ZT 8908 automatically determines the width of the data transfer at the start of each STD bus operation. Memory addresses are 32 bits wide (4 Gbytes), and I/O addresses are 16 bits wide (64 Kbytes).

SA8, SA16 — Supports 8-bit and 16-bit data transfers with STD-80 signal format and timings. The ZT 8908 automatically determines the width of the data transfer at the start of each STD bus operation. STD-80 compatible memory and I/O boards are supported.

I — Supports four additional STD bus interrupts: INTRQ1*, INTRQ2*, INTRQ3*, and INTRQ4*. These interrupts are input from the STD bus and connected to the interrupt controller through a software configurable switch. This feature is supported by the BIOS Setup program.

{MX} — Supports the multiple master (MREQx*, MAKx*) protocol. These two signals are used by the ZT 8908 in a multiple master architecture to gain control of STD bus resources. The use of these signals requires a bus arbiter, such as the ZT 89CT39, to be plugged into Slot X. The ZT 8908 requires Revision D or higher of the ZT 89CT39.

SDMA16, SDMA8 — Supports 8-bit or 16-bit Standard Architecture DMA as defined in the *STD 32 Bus Specification and Designer's Guide*. Control signals are provided through the frontplane connector.

SDMABP — Supports Standard Architecture DMA using BUSRQ*/BUSAK* for request and acknowledge and the backplane DMA control signals DMAIOR*, DMAIOW*, and T-C.

STD BUS INTERRUPTS

The ZT 8908 supports both maskable and non-maskable interrupts from the STD bus. This section discusses system level issues related to these interrupts. Refer to Chapter 4, "Interrupt Controller," for more information on the maskable interrupt controllers.

Maskable Interrupts

The STD bus maskable interrupts monitored by the ZT 8908 are INTRQ* (P44), INTRQ1* (P37), INTRQ2* (P50), INTRQ3* (E67), and INTRQ4* (P6). These maskable

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interrupts are configurable through Screen 2 of the BIOS Setup utility. Refer to Chapter 5, "Interrupt Controller," for more information.

The ZT 8908 is also capable of generating STD bus or frontplane interrupts. This feature is useful in multiple master systems to coordinate communications between processors. Typically, INTRQ4* is used for this feature in STD 32 STAR SYSTEMs.

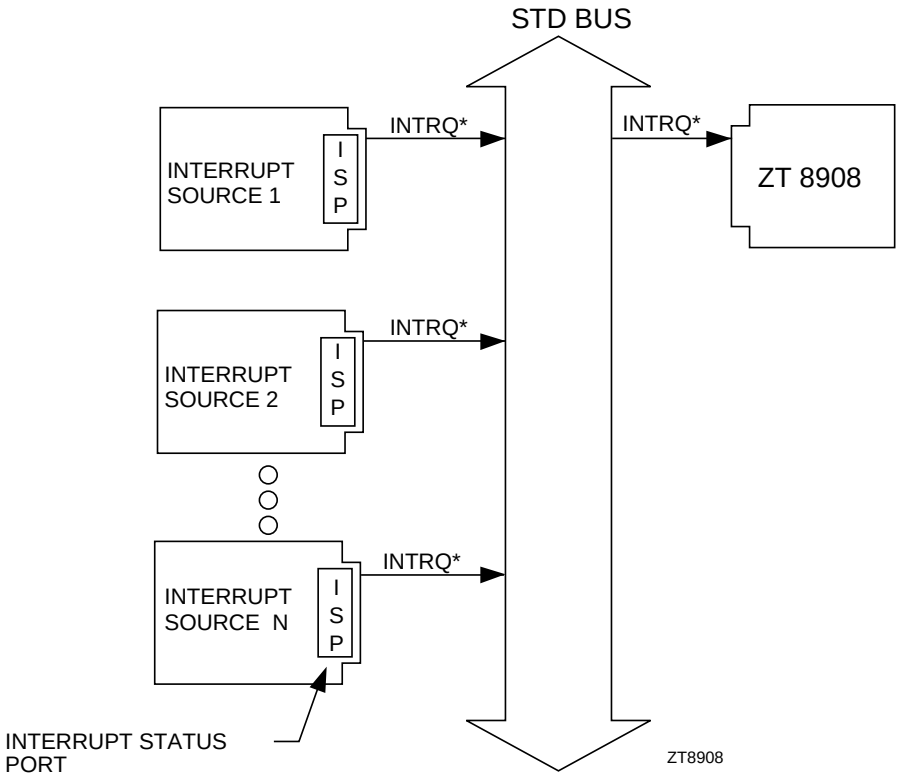
Some applications may find it necessary to share multiple interrupt sources on a single STD bus interrupt request, as shown in the "STD Bus Polled Interrupt Structure" illustration. Since the interrupt controller provides a single vector for each input, it is up to the application software to poll each possible source on the shared interrupt request signal to determine which is requesting service. This procedure is fine for most applications, provided that each source can be polled and that the interrupt controller is programmed for level-triggered operation.

Some applications include edge-triggered interrupt sources. For example, the Ziatech DOS System uses edge-triggered interrupts to support the timer used to generate the periodic system tick. Normally, the 8259 interrupt controller inputs are not independently programmable for edge-triggered or level-triggered interrupts; all inputs for these applications must be treated as edge-triggered. The ZT 8908 uses an enhanced version of the 8259 interrupt controller which does allow individual interrupt levels to be configured.

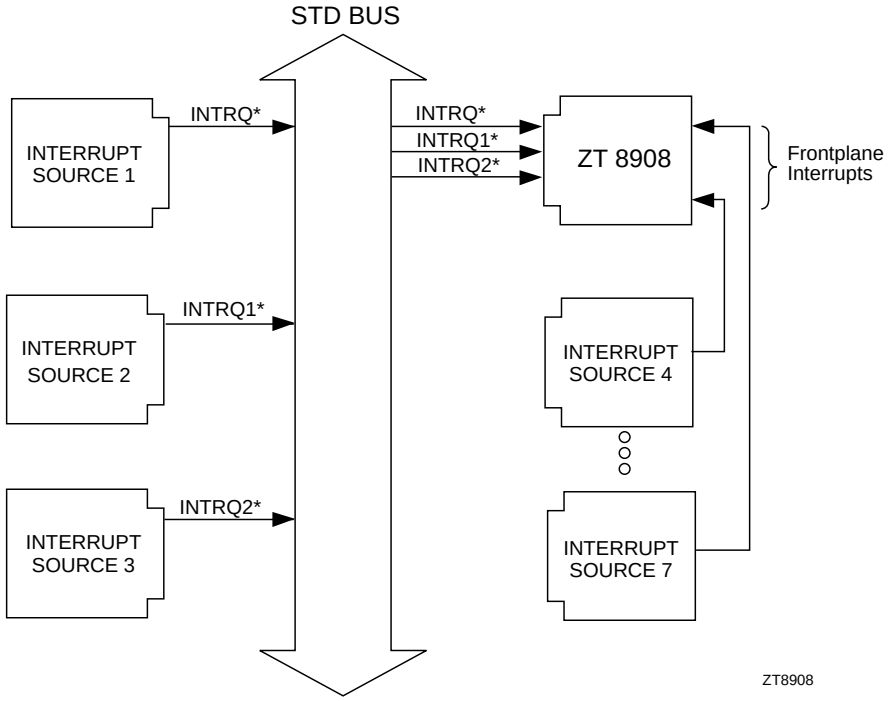
In an edge-triggered architecture, multiple interrupt sources should not share the same interrupt request signal because it is possible to miss an interrupt request from one source while an interrupt request from another source is being serviced. For this architecture, each interrupt source requires a unique connection to the interrupt controller, as shown in the "STD Bus Vectored Interrupt Structure" illustration.

The ZT 8908 can have up to 10 independent interrupt sources from off-board devices (five from the backplane, five from the frontplane). Note that normally, some of the available interrupt controller inputs are reserved for on-board use, which may limit availability for off-board peripherals. For example, if the on-board COM ports are being used, then IR3 and IR4 are not available for off-board use.

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STD Bus Polled Interrupt Structure

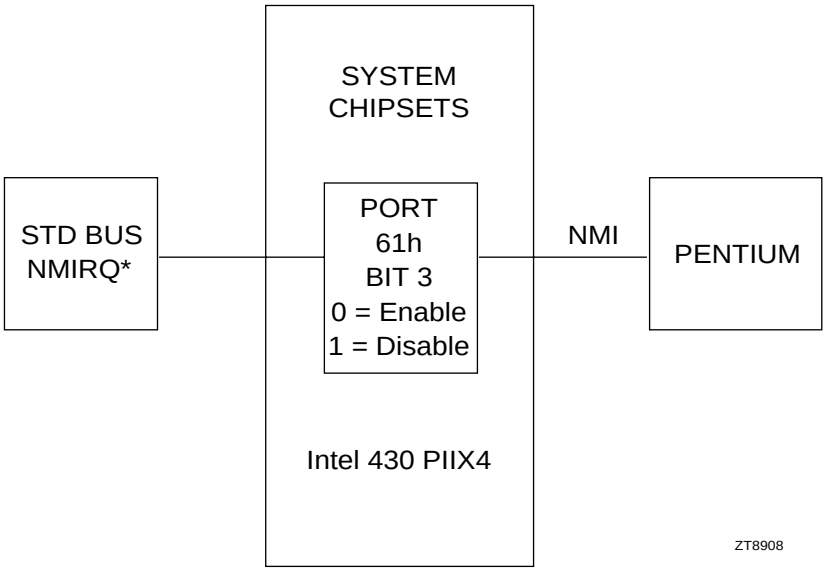


STD Bus Vectored Interrupt Structure

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Non-Maskable Interrupts

The ZT 8908 supports the STD 32 signal NMIRQ* for system errors (see the "Non-Maskable Interrupt Structure" figure). NMIRQ* is connected to the IOCHK* pin on the Intel 430 PIIX4 and is then routed to the processor.



Non-Maskable Interrupt Structure

RESET

The ZT 8908 is automatically reset with a precision voltage monitoring circuit that detects when Vcc is below the acceptable operating limit of 4.75 V. In addition, the on-board 3.3 V power supply is monitored and will reset the ZT 8908 when below 3.0 V. Other sources of reset include the watchdog timer, local pushbutton switch, and the STD bus pushbutton reset signal, PBRESET* (P48).

The ZT 8908 responds to any of these reset sources by initializing local peripherals and driving the STD bus system reset, SYSRESET* (P47). Refer to the section "Multiple Master Reset" in this chapter for more details about that environment.

MULTIPLE MASTER AND INTELLIGENT I/O

Ziatech offers two architectures for increasing the number of microprocessors in a single system: multiple master and intelligent I/O. Applications can use multiple master, intelligent I/O, or a combination of the two.

The subjects listed below are discussed in the following topics.

- Multiple Master

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- Intelligent I/O
- Multiple Master Vs. Intelligent I/O
- Multiple Master System Requirements
- Multiple Master Reset

Multiple Master

A multiple master architecture requires one permanent master and one or more temporary masters, as illustrated in the "Multiple Master Architecture" figure. The ZT 8908 is configurable for either permanent or temporary master operation (by configuring resistor packs RP59 and RP66). Each master has complete access to STD bus resources and operates at full speed when the local CPU is communicating with local memory and I/O. It is not until the application software attempts an STD bus access that arbitration occurs.

The ZT 8908 responds to an STD bus access from the application software by generating an STD bus request, MREQx* (E70), to an external bus arbiter, such as the ZT 89CT39. The ZT 89CT39 must be Revision D or higher. The ZT 8908 then suspends all local operation until the bus arbiter returns an STD bus acknowledge, MAKx* (E69). All arbitration is done in hardware on the external bus arbiter board and is transparent to the application software. The amount of time required for this arbitration depends on the amount of time higher priority masters are in control of STD bus resources. A shared resource locking mechanism is supported to guarantee exclusive access to STD bus memory or I/O.

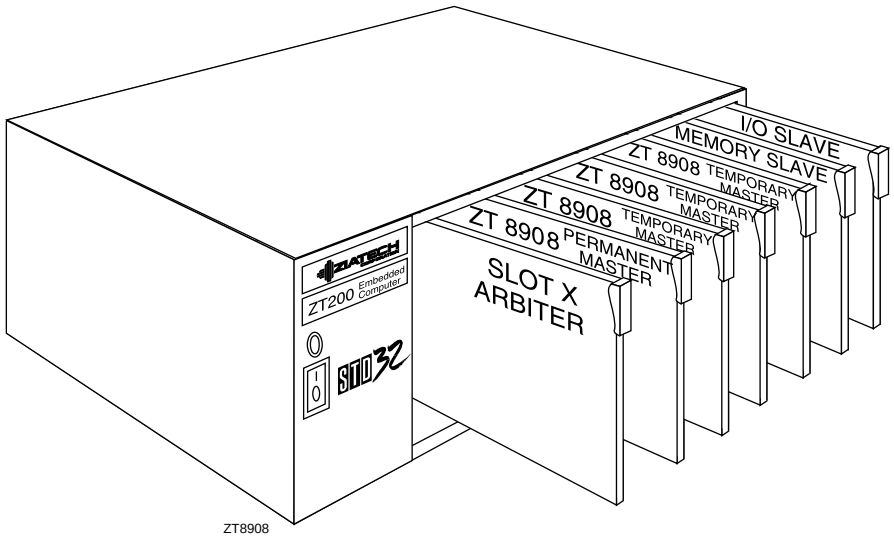
Intelligent I/O

An intelligent I/O system includes a single ZT 8908 and one or more intelligent I/O boards, such as the ZT 8832. This architecture is illustrated in the "Intelligent I/O Architecture" figure. The intelligent I/O board incorporates several I/O devices, a dual-port RAM for processor communications, and a CPU dedicated to controlling these devices.

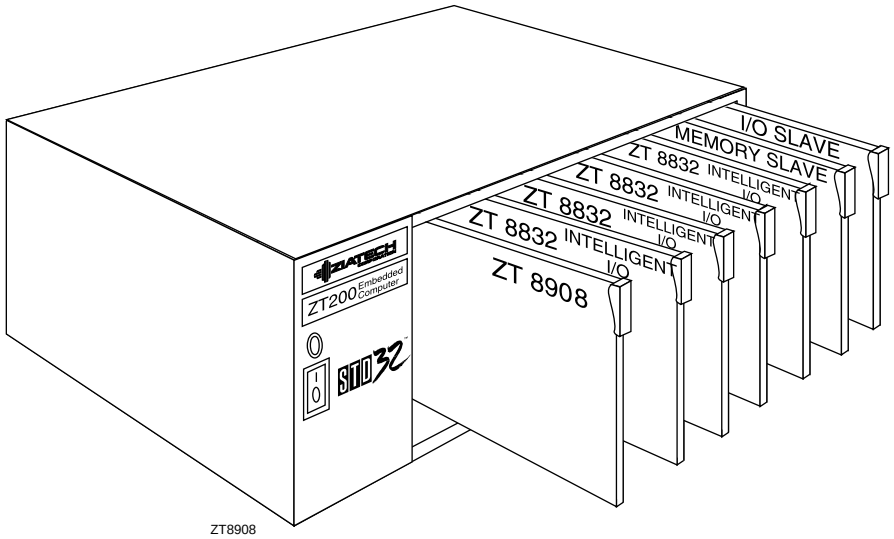
Each intelligent I/O board operates at full speed when communicating with local memory, local I/O, and dual-port RAM. The ZT 8908 also operates at full STD bus speeds when accessing the dual-port RAM. It is not until the ZT 8908 and the intelligent I/O board access the dual-port RAM at the same time that arbitration occurs.

All arbitration is done in hardware local to each intelligent I/O board, eliminating the need for an external bus arbiter. The arbitration is transparent to the application software. The amount of time required for arbitration depends on the amount of time the device in control of the dual-port RAM requires to complete operation. A shared resource locking mechanism is supported to guarantee exclusive access to dual-port RAM by either the ZT 8908 or the intelligent I/O board.

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Multiple Master Architecture



Intelligent I/O Architecture

Multiple Master Vs. Intelligent I/O

Both multiple master and intelligent I/O architectures are excellent methods of increasing system performance. The application designer has the freedom to select either architecture or combine both to meet the needs of the specific application. The following is a brief comparison of the multiple master and intelligent I/O architectures.

- An advantage of the multiple master system is that each ZT 8908 has complete access to all STD bus memory and I/O resources. In an intelligent I/O system, only the ZT 8908 has access to STD bus memory and I/O, including the dual-port RAM interface to each intelligent I/O board.

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- An advantage of the intelligent I/O system is lower system cost. The intelligent I/O architecture operates in both STD-80 and STD 32 bus structures. Dual port RAM arbitration is local to each intelligent I/O board, eliminating the need for a system arbiter. Also, most multiple master implementations require an STD bus memory slave for communications between the masters. With an intelligent I/O architecture, all communications between the single master and the intelligent I/O boards are through the dual-port RAM local to each intelligent I/O board.

Multiple Master System Requirements

The following is a list of considerations for a ZT 8908 operating in a multiple master architecture.

- One ZT 8908 must be configured as a permanent master, or there must be another permanent master in the system. The permanent master is responsible for managing the STD bus clock, CLOCK* (P49), and the system reset, SYSRESET* (P47). The remaining ZT 8908 boards must be configured for temporary master operation.

- To configure the ZT 8908 for permanent or temporary mode, two socketed resistor packs, RP59 and RP66, are used. Installing these resistor packs configures the ZT 8908 for permanent master operation (default); removing them configures the ZT 8908 for temporary master operation. RP59 and RP66 also provide pullup resistors for the SA open collector signals on the STD 32 backplane. As there can be only one master that provides the pullup mechanism, it is logical to always have the permanent master provide this feature. RP59 and RP66 are located near the gold STD 32 P/E backplane connector.

- An STD 32 backplane is required.

- A ZT 89CT39 (or equivalent) bus arbiter is needed to manage ZT 8908 access to the STD bus resources. If the ZT 89CT39 is used, it must be Revision D or higher.

- If a local PCI VGA interface is not used in multiple master operation and an STD 32 shared VGA is used, a ZT 96048 emulation RAM module must be loaded in Memory Socket U14 to retain video memory when the ZT 8908 is switched away from the backplane VGA device.

Multiple Master Reset

In a multiple master system, a ZT 8908 configured as a permanent master operates the same as a ZT 8908 operating in a single master architecture. The permanent master monitors Vcc with a precision voltage monitoring circuit and holds the system in reset when Vcc is below 4.75 V. The permanent master also will hold the system in reset when either the on-board pushbutton reset is asserted or the STD 32 bus signal PBRESET* (P48) is asserted. The permanent master asserts SYSRESET* (P47) to hold the system in reset.

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A ZT 8908 configured as a temporary master manages reset differently. A temporary master does not monitor PBRESET* and does not generate SYSRESET*. Instead, a temporary master ignores PBRESET* and monitors SYSRESET*. This enables the temporary masters to be reset when the permanent master generates SYSRESET*. This also enables the pushbutton reset on the temporary master to reset only the temporary master, while the pushbutton on the permanent master resets the entire system.

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4. INTERRUPT CONTROLLER

The ZT 8908 includes two Intel-compatible 8259 cascaded interrupt controllers incorporated into the Intel PIIX4 (82371AB) chipset that provide a programmable interface between interrupt-generating peripherals and the CPU. The interrupt controllers monitor 15 interrupts with programmable priority. When peripherals request service, the interrupt controller interrupts the CPU with a pointer to a service routine for the highest priority device.

Note: The ZT 8908 does not support cascaded interrupt controllers on the STD bus or slot-specific interrupts.

It may be helpful before using this chapter to review Chapter 3, "STD 32 Bus Interface," for a discussion on the STD-80 and STD 32 architectures and their effect on the operation of the ZT 8908.

The major features of the interrupt architecture are listed below.

- Fixed or rotating priorities
- Jumperless configuration
- PCI Interrupt support
- 15 individually maskable interrupts
- PCI Extended Mode register support
- Level-triggered or edge-triggered recognition

The interrupt architecture is presented in the "Interrupt Architecture" table. Interrupt configuration is performed through Screen 2 of the BIOS Setup utility, allowing the user to set up the interrupt architecture to the needs of the application. The Setup utility allows most of the interrupt controller interrupts to be configured from a variety of interrupt sources. The ZT 8908 supports the Extended Mode register, which allows individual programming of low-level triggered or active high-edge triggered interrupts.

Note: The message "Warning: No PCI Interrupts Available" may appear at boot time. This is because the default configuration allocates no interrupts as PCI interrupts. You may ignore this message if you are not using USB devices and if no interrupts are needed for the optional PCI mezzanine device. PCI interrupts may be allocated through the BIOS Setup utility. Any of the interrupts IR10-IR12 can be set to PCI. See the "Setup" topic in Chapter 2 for more information.

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Interrupt Architecture

Notes	CPU Interrupt	Programmable Interrupt Sources (default in bold)
1	IRQ0	**System Timer 0**
2	IRQ1	**Local keyboard** or **INTRQ1***
3	IRQ2	**Cascade**
2	IRQ3	**COM2**
2	IRQ4	**COM1**
2	IRQ5	**INTRQ4***
2	IRQ6	**INTRQ2***
2	IRQ7	**Local LPT**
4	IRQ8	**Real-Time Clock**
2	IRQ9	**INTRQ***
2	IRQ10	**J6, pin 4** or PCI
2	IRQ11	**J6, pin 6** or PCI
2	IRQ12	**J6, pin 10** or PCI
5	IRQ13	**Math Coprocessor**
2, 6	IRQ14	**INTRQ3*** or Local IDE
7	IRQ15	**J6, pin 8** or INTS

Notes:

1. CTC1-Ch0: System Timer.
2. Also supports INTRQ*****, INTRQ1***** INTRQ2*****, INTRQ3*****, INTRQ4*****, and J6--pins 2, 4, 6, 8, 10.
3. Second interrupt controller (8259).
4. Real Time Clock interrupt.
5. Math coprocessor exception interrupt.
6. Enable the ZT 8908 for either local IDE or STD 32 IDE operation through the BIOS Setup utility. See "Selecting IDE Operation Type" in Chapter 10 for details.

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7. The default IRQ15 source depends on the status of cuttable trace CT45 (see Appendix A). Other interrupt sources are possible for IRQ15 with custom software configuration. Contact Ziatech.

INTERRUPT SOURCES

The interrupt sources are summarized below. Interrupt configuration is performed through Screen 2 of the BIOS Setup utility.

Backplane: There are five STD bus interrupts routed to the interrupt configuration selection logic located in the PCI-STD Bridge. These interrupts are labeled INTRQ*, INTRQ1*, INTRQ2*, INTRQ3*, and INTRQ4*. These interrupts are active-low on the STD bus and inverted before they reach the interrupt configuration logic. Use the BIOS Setup utility to rout these interrupts to individual interrupts on the CPU.

Frontplane: All five frontplane interrupts are routed to the interrupt configuration logic. These interrupts are available through frontplane interrupt connector J6 as active-low inputs that are inverted before reaching the interrupt configuration logic. Pin assignments for connector J6 are given in the "J6 (Frontplane Interrupt Connector) Pinout" table. Use the BIOS Setup utility to rout these interrupts to individual interrupts on the CPU.

PCI: The four interrupt levels IR10, IR11, and IR12 may be assigned to the PCI bus when not used for other devices. Use the BIOS Setup utility to select the desired interrupts for PCI devices as needed.

Local: Local interrupt sources include the keyboard controller, serial ports (COM1, COM2), multiprocessor communications, IEEE Std 1284 parallel port, real-time clock, DMA controller, math coprocessor, watchdog timer, and optional IDE controller. Use the BIOS Setup utility to rout these interrupts to individual interrupts on the CPU.

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PROGRAMMABLE REGISTERS

Each interrupt controller includes four initialization registers, three control registers, and three status registers. The I/O port addressing for the interrupt controllers is given in the "Interrupt Controller Register Addressing" table. The base address of the master interrupt controller is 20h and the base address of the slave interrupt controller is A0h.

Interrupt Controller Register Addressing

Address	Register	Operation
Base+0h	IRR, ISR, IPR	Read
Base+0h	ICW1	Write
Base+0h	OCW2, OCW3	Write
Base+1h	OCW1	Read/Write
Base+1h	ICW2, ICW3, ICW4	Write

ADDITIONAL INFORMATION

- Refer to the *Ziatech Industrial BIOS for CompactPCI and STD 32 Systems* software manual for more information on the operating system's use of the interrupt inputs.
- Refer to the Intel *82371AB PCI-to-ISA/IDE Xcelerator PIIX4* data sheet for more information on the PIIX4 interrupt controller registers.

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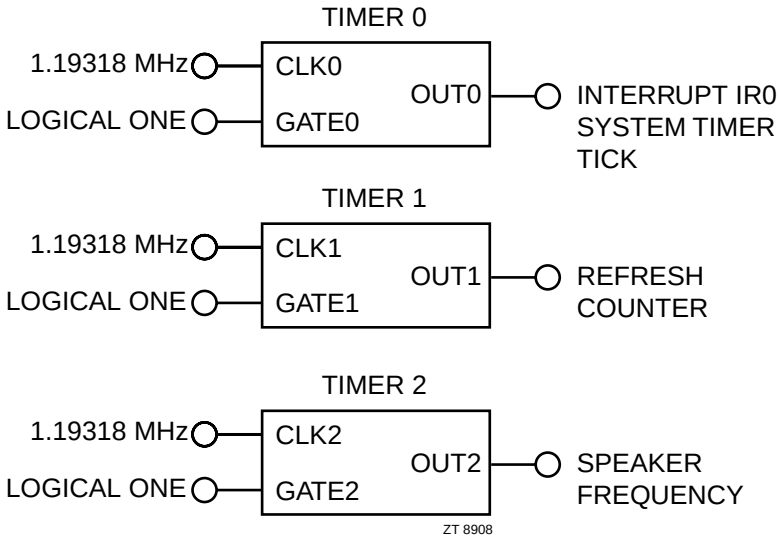
5. COUNTER/TIMERS

The ZT 8908 includes one Intel-compatible 8254 device with a total of three programmable counter/timers, incorporated into the Intel PIIX4 (82371AB) chipset. The counter/timers are useful for software timing loops, timed interrupts, and periodic interrupts. The major features of the counter/timers are listed below.

- Three 16-bit counter/timers
- Six programmable operating modes
- Binary and BCD counting
- Interrupt and polled operation

The counter/timer architecture is illustrated in the "Counter/Timer Architecture" figure. In some cases not all counter/timers are available for application development. In an MS DOS system, for example, counter/timer 0 generates a periodic system interrupt and should not be programmed by the application. Refer to the particular operating system manual for more information.

The six programmable operating modes are summarized in the "Counter/Timer Operating Modes" table.



Counter/Timer Architecture

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Counter/Timer Operating Modes

Mode	Counter/Timer Output Operation
0	Transitions after programmed count expires. Gate tied high to enable counting.
1	Transitions after programmed count expires. Gate tied high to enable counting.
2	Periodic single pulse after programmed count expires. Gate tied high to enable counting
3	Square wave with frequency equal to programmed count. Gate tied high to enable counting.
4	Single pulse after programmed count expires. Gate tied high to enable counting.
5	Single pulse after programmed count expires. Gate tied high to enable counting.

PROGRAMMABLE REGISTERS

The counter/timers are accessed through four I/O addresses, as shown in the "Counter/Timer Register Addressing" table. Each counter/timer occupies an I/O port address through which the preset count values are written and both the count and status information is read. The Control register occupies the remaining I/O port address, which services all three counter/timers.

Counter/Timer Register Addressing

Address	Register	Operation
0040h	Channel 0 Count	Read/Write
0040h	Channel 0 Status	Read
0041h	Channel 1 Count	Read/Write
0041h	Channel 1 Status	Read
0042h	Channel 2 Count	Read/Write
0042h	Channel 2 Status	Read
0043h	Control	Write

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ADDITIONAL INFORMATION

- Refer to the *Ziatech Industrial BIOS for CompactPCI and STD 32 Systems* software manual for more information on the operating system's use of the counter/timers.
- Refer to the Intel *82371AB PCI-to-ISA/IDE Xcelerator PIIX4* data sheet for more information on the PIIX4 counter/timer operating modes.

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6. DMA CONTROLLER

This chapter provides an overview of ZT 8908 DMA architecture and DMA controller operation. Illustrations of DMA controller programmable registers are also included.

ZT 8908 SPECIFICS

The ZT 8908 includes two cascaded, Intel-compatible, 8237 Direct Memory Access controllers that provide a programmable interface for direct transfers between peripherals and main memory. Seven channels of DMA are supported, with up to four devices located on the STD 32 bus. The DMA controllers used on the ZT 8908 are supersets of the 8237 device incorporated into the Intel PIIX4 (82371AB) chipset, supporting 32-bit memory accesses, higher speed transfers, and the PCI protocol. Features of the DMA controllers include:

- PCI bus mastering
- Fixed or rotating priorities
- 8237 compatible/superset
- Compatible, TYPE A, TYPE B, TYPE F transfer rates
- Seven DMA channel support
- 32-bit memory addressing

The DMA architecture is illustrated in the "DMA Architecture" figure.

DMA CHANNELS

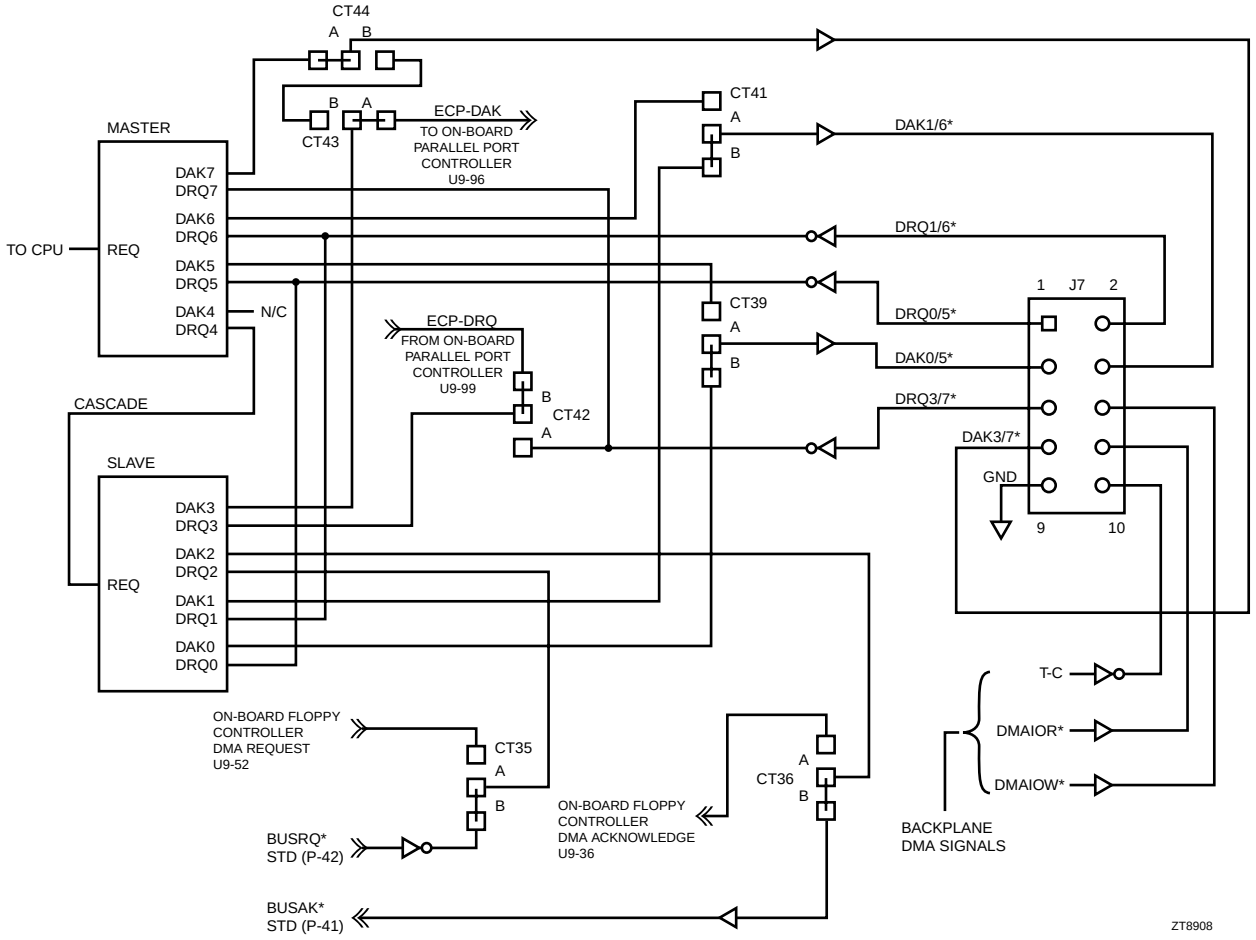
The DMA channels are summarized below. The channels are configurable through Screen 2 of the BIOS Setup utility.

Backplane: DMA service is available for the BUSRQ*/BUSAK signals on the STD 32 backplane. Normally, these signals are used for servicing a backplane floppy disk controller via DMA Channel 2. If a floppy disk controller is not used, the system is configurable to allow servicing of BUSRQ*/BUSAK* by DMA Channel 5 for 16-bit peripherals. If a floppy disk controller is used, only DMA Channel 2 is allowed for BUSRQ*/BUSAK*.

Frontplane: Four channels of DMA are supported through the frontplane DMA connector (J7). The four channels are independently selectable (through cuttable traces CT37, CT39, CT41-CT44) for 8-bit or 16-bit operation. Channels 0, 1, 5, and 6 can be used by STD 32 peripherals for DMA servicing.

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Local: The on-board IEEE Std 1234 Parallel Port (see Chapter 10) can be configured to use DMA channel 0 for data transfers. The Parallel Port must be configured for ECP mode to use DMA.



DMA Architecture

PROGRAMMABLE REGISTERS

Each DMA controller is managed through the 16 I/O port addresses shown in the "Slave DMA I/O Port Addressing" table. Page registers extend the 16-bit DMA address to the full 24-bit address space available on the ZT 8908. I/O port addressing for the DMA page registers is given in the "DMA Page I/O Port Addressing" and "DMA Extended Page (A24-31) I/O Port Addressing" tables.

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Slave DMA I/O Port Addressing

Address			
Slave	**Master**	**Register**	**Operation**
0	C0	Channel 0 Base/Current Address	Write
		Channel 0 Current Address	Read
1	C2	Channel 0 Base/Current Count	Write
		Channel 0 Current Count	Read
2	C4	Channel 1 Base/Current Address	Write
		Channel 1 Current Address	Read
3	C6	Channel 1 Base/Current Count	Write
		Channel 1 Current Count	Read
4	C8	Channel 2 Base/Current Address	Write
		Channel 2 Current Address	Read
5	CA	Channel 2 Base/Current Count	Write
		Channel 2 Current Count	Read
6	CC	Channel 3 Base/Current Address	Write
		Channel 3 Current Address	Read
7	CE	Channel 3 Base/Current Count	Write
		Channel 3 Current Count	Read
8	D0	Status	Read
		Command	Write
9	D2	Write Request	Write
A	D4	Write Single Mask	Write
B	D6	Write Mode	Write
C	D8	Clear Byte Pointer	Write
D	DA	Clear Master	Write
E	DC	Clear Mask	Write
F	DE	Write Mask	Write

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DMA Page I/O Port Addressing

Address	Register	Operation
87h	Channel 0 A16-23 Address	Read/Write
83h	Channel 1 A16-23 Address	Read/Write
81h	Channel 2 A16-23 Address	Read/Write
81h	Channel 2 A16-23 Address	Read/Write
82h	Channel 3 A16-23 Address	Read/Write
8Bh	Channel 5 A16-23 Address	Read/Write
89h	Channel 6 A16-23 Address	Read/Write
8Ah	Channel 7 A16-23 Address	Read/Write

DMA Extended Page (A24-31) I/O Port Addressing

Address	Register	Operation
487h	Channel 0 A24-31 Address	Read/Write
483h	Channel 1 A24-31 Address	Read/Write
481h	Channel 2 A24-31 Address	Read/Write
481h	Channel 3 A24-31 Address	Read/Write
48Bh	Channel 5 A24-31 Address	Read/Write
489h	Channel 6 A24-31 Address	Read/Write
48Ah	Channel 7 A24-31 Address	Read/Write

ADDITIONAL INFORMATION

- Refer to the *Ziatech Industrial BIOS for CompactPCI and STD 32 Systems* software manual for more information on the operating system's use of the interrupt inputs.
- Refer to the Intel *82371AB PCI-to-ISA/IDE Xcelerator PIIX4* data sheet for more information on the PIIX4 DMA controller operating modes. The data sheet is available online at:

  http://developer.intel.com/design/chipsets/datashts/290550.htm
- Refer to the National Semiconductor® *PC87309 SuperI/O™ Plug and Play Compatible Chip in Compact 100-Pin VLJ Packaging* data sheet for more

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information on configuring the ECP DMA channel. The data sheet is available online at:

http://www.national.com/ds/PC/PC87309.pdf

These data sheets are in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com.

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7. REAL-TIME CLOCK

The ZT 8908 includes one Motorola-compatible 146818 real-time clock incorporated into the Intel PIIX4 (82371AB) chipset. The real-time clock provides clock and 100-year calendar information in addition to 256 bytes of CMOS setup static RAM. These functions are battery backed for continuous operation even in the absence of system power. The RAM is used by the operating system BIOS to store configuration information. The major features of the real-time clock are listed below.

- Battery backed
- Year 2000 Compliant
- Leap year compensation
- 50 bytes of CMOS setup RAM
- Periodic, Alarm, and Update Ended interrupts
- Timekeeping to a 1 second resolution
- Daylight Savings Time compensation

PROGRAMMABLE REGISTERS

The real-time clock includes 64 register locations. These registers are accessed through I/O port locations 70h and 71h. A real-time clock register is accessed by first writing the offset address of the register to I/O port location 70h. Data is then transferred to or from the register through I/O port location 71h. This sequence must be repeated to read the same register a second time. The I/O port addressing for the real-time clock is given in the "Real-Time Clock Register Addressing" table.

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Real-Time Clock Register Addressing

Address Offset	Function	Range
0h	Time-Seconds	0-59
1h	Alarm-Seconds	0-59
2h	Time-Minutes	0-59
3h	Alarm-Minutes	0-59
4h	Time-Hours (12 hour mode)	1-12
4h	Time-Hours (24 hour mode)	0-23
5h	Alarm-Hours	0-23
6h	Day of Week	1-7
7h	Date of Month	1-31
8h	Month	1-12
9h	Year	0-99
Ah-Dh	Register A-D	—
Eh-3Fh	General Purpose	—

ADDITIONAL INFORMATION

Refer to the Intel *82371AB PCI-to-ISA/IDE Xcelerator PIIX4* data sheet for more information on the real-time clock operating modes.

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8. SERIAL CONTROLLER

This chapter discusses operation of the ZT 8908's two serial ports. Each channel is compatible with the industry standard 16550 serial port, including support for a 16 byte FIFO for read and write operations.

SPECIFICS

The ZT 8908 includes two serial ports that are compatible with the industry standard 16550. The drivers for each serial port are implemented with 5 V charge pump technology. The serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115.2 Kbaud. Both channels are supplied as DTE configured devices through the multi-I/O connector (J4). The ZT 90243 Multi-I/O cable allows each channel to interface directly to 9-pin D-Shell serial devices, as used in PC applications. Each port may be disabled to allow for STD 32 based COM ports (such as an off-board modem) to be used.

The major features of each serial port are listed below.

- 16550 compatible
- Loopback diagnostics
- Two RS-232 channels
- Baud rates up to 115.2 Kbaud
- Polled and interrupt operation
- Drivers do not require ±12 V

Details for the two serial ports on the ZT 8908 are discussed in the following topics.

Address Mapping

The address mapping for the PC standard architecture and the ZT 8908 is shown below.

Serial Channel	PC Port Address	ZT 8908 Port Address
COM1	3F8-3FF	3F8-3FF or disabled for off-board COM support
COM2	2F8-2FF	2F8-2FF or disabled for off-board COM support

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Interrupt Selection

The interrupt mapping for the PC standard architecture and the ZT 8908 is shown below. Different interrupt levels for COM1 and COM2 interrupts are selectable through Screen 2 of the BIOS Setup utility.

Serial Channel	PC Interrupt	ZT 8908 Interrupt
COM1	IR4	IR4 or disabled for off-board COM support
COM2	IR3	IR3 or disabled for off-board COM support

Handshake Signals

The PC architecture includes the following signals:

- Ring Indicator (RI)
- Clear To Send (CTS)
- Receive Data (RXD)
- Transmit Data (TXD)
- Data Terminal Ready (DTR)
- Data Carrier Detect (DCD)
- Request To Send (RTS)
- Data Set Ready (DSR)

Serial Channel Interface

The serial ports are configured as DTE and are available through the 68-pin SCSI type multi-I/O connector (J4). J4 connector pin assignments are shown in the "Connectors" section of Appendix B. The optional ZT 90243 Multi-I/O cable converts the serial port interface to standard 9-pin D-shell connectors.

PROGRAMMABLE REGISTERS

There are seven registers for initializing and controlling each serial channel. The "Serial Controller Register Addressing" table shows the I/O port addressing for the COM port registers.

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Serial Controller Register Addressing

COM 1 Address	COM 2 Address	Register	Operation
03F8h (DIV=0)	02F8h (DIV=0)	Receive Buffer	Read
03F8h (DIV=0)	02F8h (DIV=0)	Transmit Buffer	Write
03F8h (DIV=1)	02F8h (DIV=1)	Divisor Latch LSB	Read/Write
03F9h (DIV=0)	02F9h (DIV=0)	Interrupt Control	Read/Write
03F9h (DIV=1)	02F9h (DIV=1)	Divisor Latch MSB	Read/Write
03FAh	02FAh	Interrupt Status	Read
03FAh (DIV=X)	02FAh (DIV=X)	FIFO Control	Write
03FBh	02FBh	Line Control	Read/Write
03FCh	02FCh	Modem Control	Read/Write
03FDh	02FDh	Line Status	Read
03FEh	02FEh	Modem Status	Read
03FFh	02FFh	Reserved	

ADDITIONAL INFORMATION

Refer to the National Semiconductor *PC87309 Super I/O™ Plug and Play Compatible Chip in Compact 100-Pin VLJ Packaging* data sheet for more information on the serial controller operating modes. The data sheet is available online at:

http://www.national.com/ds/PC/PC87309.pdf

The data sheet is in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com.

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9. IEEE STD 1284 PARALLEL PORT INTERFACE

The ZT 8908 supports an IEEE Std 1284 compatible parallel printer port interface, available through the multi-I/O connector (J4).

The printer port is configurable for Normal (compatibility), Extended (Ext), EPP, or ECP modes through Screen 2 of the BIOS Setup utility.

The ZT 90243 Multi-I/O cable allows the on-board LPT1 channel to interface directly to 25-pin D-Shell parallel port devices, as used in PC applications. The on-board port may be disabled to allow use of STD 32 based parallel interfaces.

PARALLEL PORT CONFIGURATION OPTIONS

The different modes for the printer port are described below. Details for the parallel port on the ZT 8908 are discussed in the following topics. Shown in parenthesis is the description for each of the modes as presented in Screen 2 of the BIOS Setup utility.

Parallel Port Mode	Description	Max. Data Rate
Compatibility (Normal) This is the default mode.	Uni-directional data configuration. The original PC-AT Mode. Also known as "nibble mode" because the four status bits in the cable are used for feedback from devices such as tape back-up units (when restoring data from a tape). Software based protocol.	50-150 Kbits/s
Extended (Ext)	Bi-directional data transfer capability. Similar to Normal mode, but allows 8-bit data in both directions. Faster for interfaces needing to supply data to the computer (e.g., scanners, tape back-up). Software based protocol.	50-150 Kbits/s
EPP	Enhanced Parallel Port. Hardware based handshaking of the data transfers provide single I/O instruction data transfers in read and write operations. Register superset of Normal/Extended modes.	500 Kbits/s-2 Mbits/s
ECP	IEEE Std 1284 Extended Capability Port. Similar to EPP, but register set is strictly defined. Adds FIFO's for read/write operations. ECP devices require IEEE Std 1284 compliant cabling and buffers. The ZT 8908 supplies compliant buffers - cabling is available from other sources.	500 Kbits/s-2 Mbits/s

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ADDRESS MAPPING

The address mapping for the PC standard architecture and the ZT 8908 is shown below. The on-board port may be disabled through Screen 2 of the BIOS Setup utility to allow an STD 32 LPT port to be used.

Parallel Port	PC Port Address	ZT 8908 Port Address
LPT1	3BC (typically)	378-37F - Normal, Extended, EPP Modes
		378-37A, 778-77A - ECP Mode

INTERRUPT SELECTION

The interrupt mapping for the PC standard architecture and the ZT 8908 is shown below.

Parallel Port	PC Interrupt	ZT 8908 Interrupt
LPT1	IR5	IR7 or disabled for off-board LPT support

DMA SELECTION

DMA may be configured for ECP mode in software. DMA channel 0 is dedicated for ECP support and may be used by application software. The BIOS does not use DMA for any data transfers. Applications needing DMA support must configure the parallel port with appropriate initialization code.

PROGRAMMABLE REGISTERS

There are three registers for the compatibility/extended mode parallel port interface. The "Compatibility/Extended Mode Parallel Port Interface Addressing" table shows the I/O port addressing. For EPP and ECP information, see the data sheet referenced in "Additional Information" at the end of this chapter.

Compatibility/Extended Mode Parallel Port Interface Addressing

Address	Register	Operation
0378h	Line Printer Data	Read/Write
0379h	Line Printer Status	Read
037Ah	Line Printer Control	Read/Write

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ADDITIONAL INFORMATION

Refer to the National Semiconductor *PC87309 Super I/O™ Plug and Play Compatible Chip in Compact 100-Pin VLJ Packaging* data sheet for more information on the parallel printer port controller operating modes. The data sheet is available online at:

http://www.national.com/ds/PC/PC87309.pdf

The data sheet is in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com.

The IEEE-1284 specification (document #DS02709) can be obtained from the IEEE Standards Office at (800) 678-4333.

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10. OPTIONAL IDE INTERFACE

The ZT 8908 supports a local Intelligent Drive Electronics (IDE) hard disk through an optional IDE interface connector (J8). The hard drive mounts to the bottom side of the ZT 8908 either directly or on an adapter board and is attached with three screws. This feature is useful for single board applications as well as STAR SYSTEMs where the ZT 8908 needs to have a local (non-shared) hard disk.

The specific size of the drive (in Megabytes) sold with this option may change because the hard disk drive market continually improves capacity. In general, Ziatech offers a higher capacity drive for the same or similar price when a new drive is qualified.

The onboard IDE interface is a factory load option at Ziatech. Option D1 to the ZT 8908 includes a hard disk, mounting hardware, cable, and connector. When configured for local IDE operation, the ZT 8908 requires one additional slot in the STD 32 card cage. The onboard IDE hard disk is PCI-based and will be higher performance than an STD 32 based IDE controller.

It is not possible to configure the ZT 8908 for both onboard IDE operation and STD 32 IDE operation. The ZT 8908 has a green hard disk activity light for local IDE accesses.

HARD DISK MOUNTING

The ZT 8908 has three mounting holes for the 2.5 inch IDE hard disk. A 44-pin 2 mm latching connector (J8) is also provided. The hard disk is then connected using a short 2 mm cable. This option is not field installable and must be installed at Ziatech Corporation.

SELECTING IDE OPERATION TYPE

Enable the ZT 8908 for onboard or STD 32 operation through the BIOS Setup utility. Your selection automatically configures the ZT 8908 for I/O addressing and interrupt support.

Access the utility by pressing the "**S**" key while the system is booting.

Onboard IDE Operation

In Screen 1, set the IDE Interface parameter to **ONBOARD**.

In Screen 2, set the Interrupt Request 14 parameter to **IDE**.

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STD 32 IDE Operation (default)

In Screen 1, set the IDE Interface parameter to **STD32**.

In Screen 2, set the Interrupt Request 14 parameter to **INTRQ3**.[†]

STAR SYSTEM APPLICATIONS

Certain STAR SYSTEM applications require a CPU board to have exclusive access to an IDE drive, such as when a CPU is booting a unique operating system, or when, for performance reasons, a CPU requires isolated (non-shareable) hard disk capability. All of these needs are met by using an onboard IDE interface.

Overall system performance is also improved when using an onboard IDE interface because without local IDE accesses impacting the STD 32 bus, other processors experience lower latency times to system-wide resources. Additionally, the local processor does not have to arbitrate for the STD 32 bus in order to perform local IDE transfers.

Refer to the *STD 32 STAR SYSTEM User's Manual* for more information.

SINGLE BOARD APPLICATIONS

When the ZT 8908 is used in single board applications with a local IDE hard disk, Ziatech suggests that the application provide power to the ZT 8908 via a mating STD 32 connector. For mounting support, both the STD 32 connector and standoffs (to PCB mounting holes located on the ZT 8908) should be used to physically support the assembly. This will vary depending on the application. Contact Ziatech for assistance.

[†] Note:INTRQ3* is the default mapping for ZT 8952/ZT 8953 IDE drives. If for some reason these drives have been configured to use other interrupt channels, the ZT 8908 must be set up accordingly.

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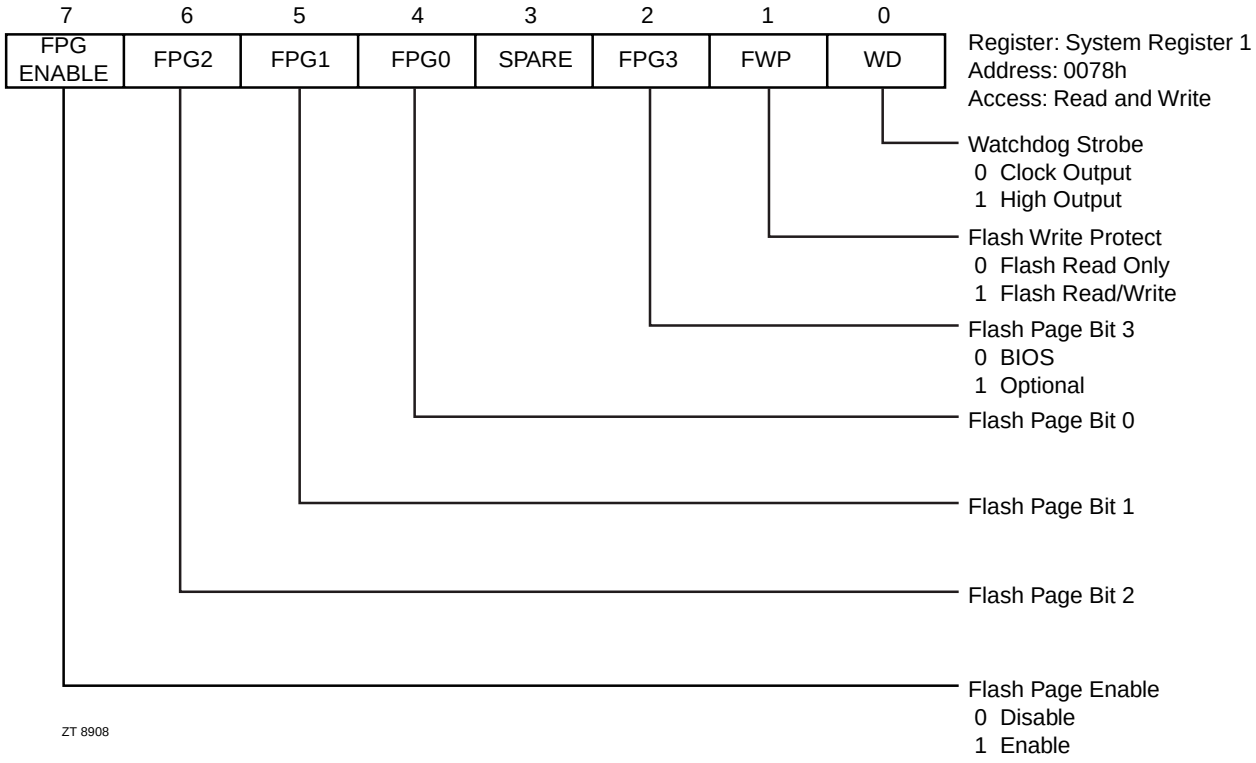
11. SYSTEM REGISTERS

Three system registers are used to control and monitor a variety of functions on the ZT 8908. These registers are located at I/O address range 0078h – 007Ah. Two of the registers are read/write capable; the third is a read-only register. Normally, only the system BIOS uses these registers, but they are documented here for application use as needed. Because the system BIOS controls (and may need to rely on the status of) certain bits in these registers, take care when modifying the contents of these registers.

PROGRAMMABLE REGISTERS

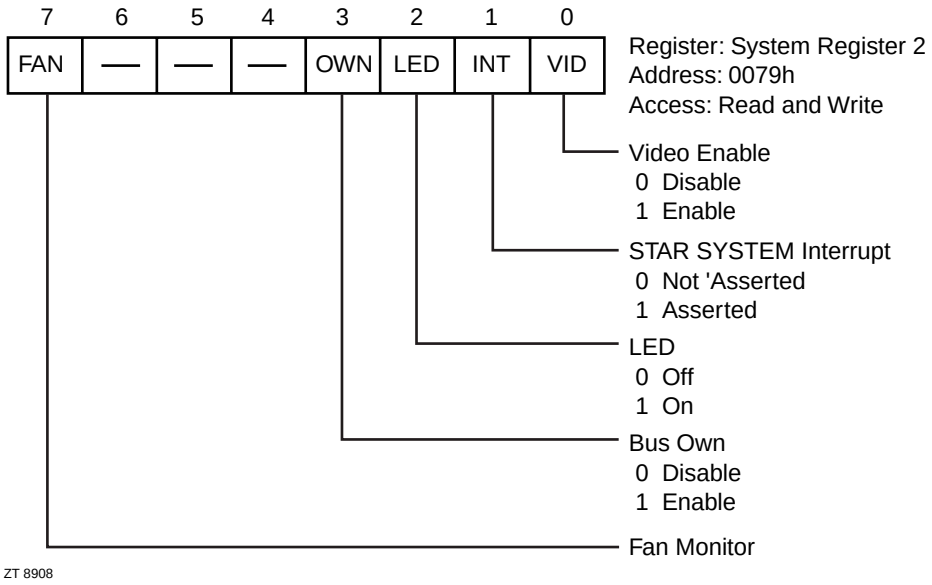
The following System registers are illustrated in this chapter:

- System Register 1
- System Register 2
- System Register 3

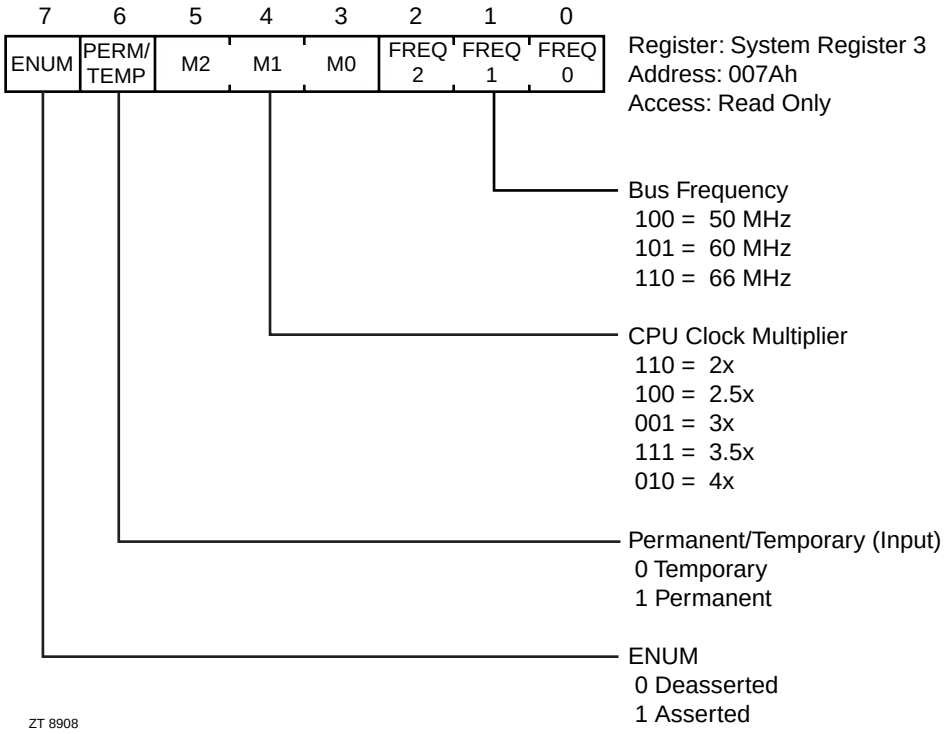


System Register 1

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System Register 2



System Register 3

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12. WATCHDOG TIMER

The primary function of the watchdog timer is to monitor ZT 8908 operation and take corrective action if the system fails to function as programmed. The major features of the watchdog timer are listed below.

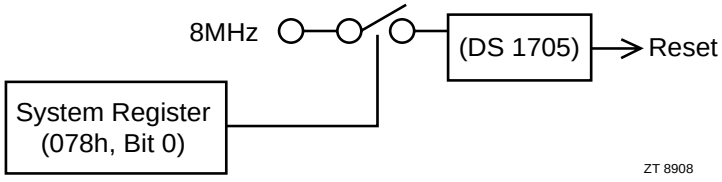
- Single-stage
- Enabled and disabled through software control
- Armed and strobed through software control

WATCHDOG TIMER OPERATION

The watchdog timer architecture is shown in the "Watchdog Timer Architecture" figure. The watchdog timer is implemented in the Dallas Semiconductor™ DS1705 system monitor.

After power on or reset, the watchdog function is disabled, meaning that the watchdog is continually being strobed by an 8 MHz signal. Bit 0 of System Register 1 (078h) must be programmed with a logical 1 to enable the watchdog timer to begin operation. If the watchdog is allowed to expire, a reset is generated. To strobe the watchdog, bit 0 of System register 1(078h) must be written with a logical 0 and then a logical 1.

The watchdog timeout period is fixed at 1.0 s minimum and 2.2 s maximum. Software must strobe the watchdog timer within 1.0 s to guarantee that the system is not reset.



Watchdog Timer Architecture

The following code shows the procedure for arming and strobing the watchdog timer.

```
;--------------------------------------
; The multiple master interrupt is
; a bi-directional bit.  The current
; software state of multiple master
; interrupt is maintained in the
; multiple master state bit. Input_e5
; updates the multiple master bit with
; the current software state maintained
```


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```
; in the multiple master state bit.
;-------------------------------------
input_e5    macro
            local     multiple_on
            in        al,0e5h
            test      al,8
            jnz       multiple_on
            and       al,not 10h
multiple_on:
            endm
;-------------------------------------------------------------
;  strobe_wd strobes and re-arms the watchdog timer.
; The state of Bit 1 must be maintained (write the same
; value as was read).
; Bits 3 & 4 must be handled as shown in the input_e5 macro
;-------------------------------------------------------------
strobe_wd   pushf
            cli
            input_e5
            and       al,not 1
            out       0e5h,al
            or        al,1
            out       0e5h,al
            popf
            ret
```

ADDITIONAL INFORMATION

Refer to the Dallas Semiconductor *DS1705/DS1706 3.3 and 5.0 V MicroMonitor™* data sheet for more information on the watchdog timer and the associated operating modes. The data sheet is available online at:

http://www.dalsemi.com/DocControl/PDFs/1705-06.pdf

The data sheet is in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com.

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13. PCI MEZZANINE LOCAL BUS

The ZT 8908 includes a PCI compatible local bus interface (J5) to industry standard PCI mezzanine devices. The bus operates at half of the CPU *external* clock speed. Ziatech offers PCI peripheral adapters designed specifically for this local bus interface. These adapters give superior performance over STD bus solutions by running with up to four times the data width and up to four times the operating frequency. Major features of the PCI interface are listed below.

- 25, 30, or 33 MHz operation (determined by CPU speed)
- Reduces STD bus traffic by keeping all PCI operations local
- Single-slot occupancy capable (VGA)

See the section, "Removing The zPM Mezzanine Card," in Chapter 2 for details about the mechanical connection of mezzanine devices to Ziatech CPUs.

PCI OPERATION FREQUENCY

The PCI operating frequency is derived from the frequency at which the AMD-K6 or Pentium processor is operating. Both processors are available with several different internal clock multipliers.

Processor Speed (MHz)	Internal Clock Multiplier	External Processor Speed	PCI Operating Frequency
133	2.0X	66.6	33.3
233 (Intel MMX)	3.5X	66.6	33.3
266 (K6 MMX)	4.0X	66.6	33.3

ADDITIONAL INFORMATION

Refer to the individual peripheral data sheets for additional details and for installation and operating instructions.

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14. PROGRAMMABLE LED

The ZT 8908 includes two Light-Emitting Diodes (LEDs). A green LED for the optional IDE disk drive is mounted on the solder side of the board near the multi-I/O connector (J4). A red general purpose LED is located just under the extractor. The red LED is software programmable through bit 2 in System Register 2. Writing a logical 0 to bit 2 turns the LED off; writing a logical 1 turns the LED on. The LED is turned off after a power cycle or a reset.

Because the LED bit is in the same register as several system level functions, it is important to preserve the state of the other bits in this register when modifying the LED status. The following code demonstrates the mechanism for modifying the LED bit.

```
;  turn LED ON
cli                     ; clear interrupts
in     al, 79h          ; read current state
or     al, 04h          ; set LED bit
out    79h, al          ; output new value for register
sti                     ; re-enable interrupts


;  turn LED OFF
cli                     ; clear interrupts
in     al, 79h          ; read current state
and    al, not 04h      ; clear LED bit
out    79h, al          ; output new value for register
sti                     ; re-enable interrupts
```


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15. THERMAL CONSIDERATIONS

The ZT 8908 comes from the factory with an integrated fan/heatsink (available through connector J2) for cooling the processor. The fan/sink allows a maximum ambient air temperature between 0º C and 70º C, depending on the speed of the processor (70º C maximum case temperature). The values in the figures and tables referenced below are stress ratings only. Do not operate the ZT 8908 at these maximums. See the "DC Operating Characteristics" section in Appendix B for operating conditions.

See the following figures and tables.[†]

- "Ambient Temperature Vs. Pentium Processor Case Temperature" figure
- "AMD-K6 Processor Maximum Ambient Temperature" table
- "Pentium Processor Maximum Ambient Temperature" table

Pentium Processor Maximum Ambient Temperature

Processor Speed (MHz)	Max. Ambient Temperature (°C)
133	56
233 (MMX)	49

AMD-K6 Processor Maximum Ambient Temperature

Processor Speed (MHz)	Max. Ambient Temperature (°C)
266 (MMX)	50

TACHOMETER MONITORING

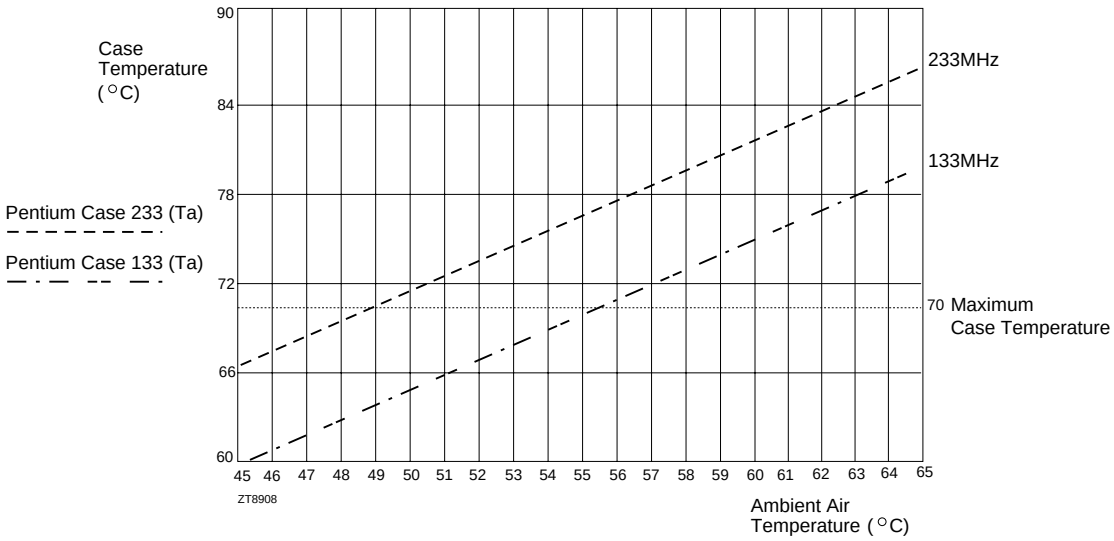
The ZT 8908 has optional circuitry on board for monitoring a fan with a tachometer output.[‡] The tachometer input is connected to J2, pin 3. The input circuitry, shown in the "Tachometer Monitoring Input Circuitry" figure, contains a two-resistor voltage divider (R29, R30) and a protection diode (D3) to allow for a +12 V tachometer signal. The tachometer signal connects to System register 2, bit 7 at I/O port 0079h. Since this input is directly connected to the tachometer, user-written software is necessary to determine if the fan is working properly. Most fan tachometers have an output rate of approximately 100 Hz; this input therefore changes states approximately every 5 ms.

[†] Contact Ziatech for Ambient Temperature Vs. AMD-K6 Processor (MMX) Case Temperature information

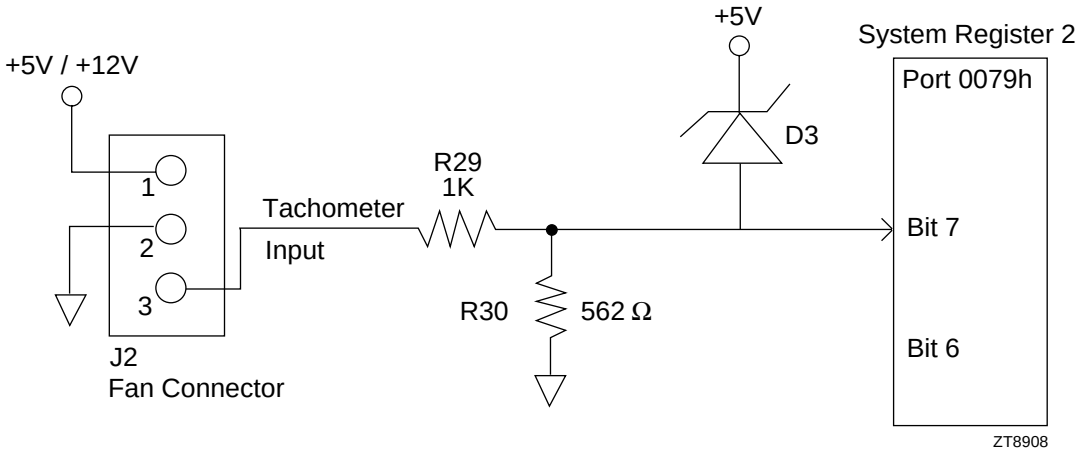
[‡] This feature is not implemented on the ZT 8908A release of the product.

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Note: The factory installed fan/sink **does not** have a tachometer output.



Ambient Temperature Vs. Pentium Processor Case Temperature



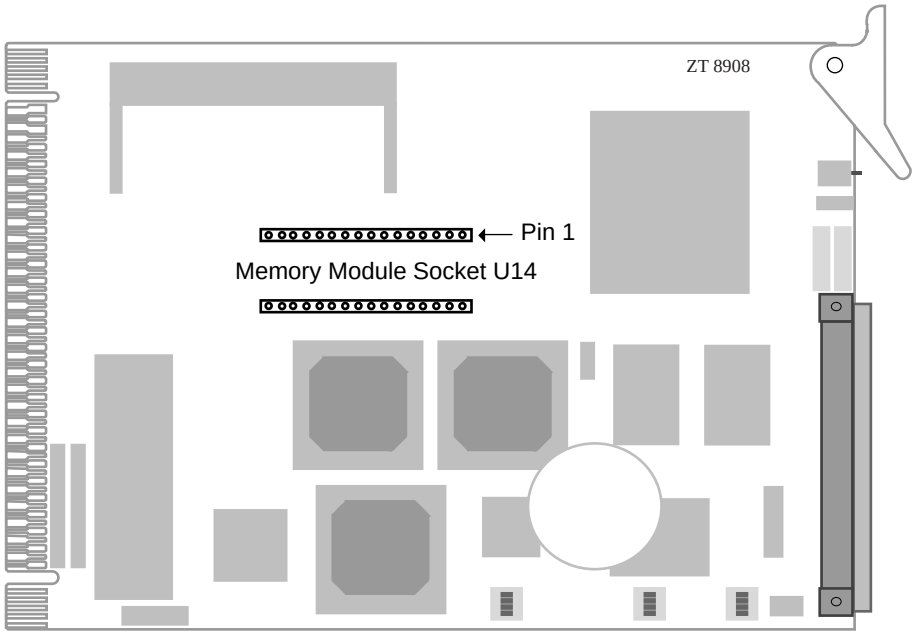
Tachometer Monitoring Input Circuitry

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16. MEMORY SOCKET (U14)

The ZT 8908's memory socket (U14) has two functions, configurable through DIP switches SW1-1 and SW1-3. The functions are listed below and discussed in the following topics.

- BIOS Recovery
- STAR SYSTEM Video Emulation SRAM



Memory Socket (U14)

BIOS RECOVERY

If the ZT 8908's BIOS becomes corrupted, recover it by installing a BIOS Recovery Device (ZT 95207) into the memory socket (U14). This device allows the board to boot so the BIOS can be reflashed. To order the BIOS Recovery Device, contact Ziatech.

The steps below explain how to boot from the boot socket and reflash the BIOS. For more details, see the *Ziatech Industrial Computer System Manual for BIOS Version 4*, or refer to the Tech. Briefs maintained on Ziatech's FTP site located at http://www.ziatech.com/techbriefs.htm.

1. Power off the system and remove the ZT 8908 from the card cage.

2. Close SW1-3 to enable the BIOS Recovery Device.

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3. Open SW2-1 to disable flash write protection.

4. Insert the BIOS Recovery Device into the boot socket. Make sure the device is correctly oriented.

5. Reinstall the ZT 8908 into the card cage and reboot the system. The CPU will boot either to a Mini Command colon prompt (:) or a P: prompt if the P: drive contents are still intact.

6. To reflash the BIOS:

   a) Insert the STD 32 Development Software diskette (ZT 97137) into the floppy drive.

   b) Type

   ```
   A:\UTIL\FLASH /B A:\IMAGES\SYS8908.B00
   ```

   or

   ```
   A:\UTIL\FLASH /B A:\IMAGES\SYS8908M.B00
   ```

   depending on whether you are recovering a STAR BIOS image or a standard BIOS image. An **M** at the end of the filename indicates STAR BIOS; no **M** indicates standard BIOS. Type the **"Y"** key to respond to the warning messages and the BIOS will be reflashed.

7. After reflashing the BIOS, power off the system and remove the ZT 8908 from the card cage.

8. Remove the BIOS Recovery Device from socket U14 and open SW1-3.

STAR SYSTEM VIDEO EMULATION SRAM

When the ZT 8908 is used in a STAR SYSTEM and sharing a video card with other CPUs, a 128 Kbyte SRAM module must be installed in socket U14. Perform the steps below.

1. Power off the system and remove the ZT 8908 from the card cage.

2. Close SW1-1 to enable the video RAM region when the system re-boots.

3. Install a 128 Kbyte SRAM module into socket U14. Make sure the device is correctly oriented.

4. Reinstall the ZT 8908 into the card cage and reboot the system.

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A. BOARD CONFIGURATION

The ZT 8908 includes several options that tailor the operation of the board to requirements of specific applications. Most of the options are selected through the BIOS Setup utility. Some options cannot be software controlled and are configured with switches or cuttable traces. Switch options are made by opening or closing the desired switch. Cuttable trace options are made by installing and removing surface mount 0 Ω resistors.

This appendix is organized according to the three types of configuration options: BIOS Setup, switches, and cuttable traces. It also provides illustrations of the board showing the locations of switches and cuttable traces.

CPU SETUP AND OPERATION

Your ZT 8908 is configured at the factory for the specific processor installed. Each processor has its own setup configuration and should only be changed by Ziatech.



Warning: Changing the processor to a type other than the one installed by Ziatech may damage the processor and other devices on the ZT 8908.

DRAM INSTALLATION AND REMOVAL OVERVIEW

The ZT 8908 requires two identical 72-Pin SO-DIMM modules for proper operation. The correct DRAM modules have been installed by the factory and in most cases should not need to be changed.



Warning: Installing DRAM modules other than those qualified by Ziatech may cause the board to operate intermittently.

The following two topics describe how to remove and install the DRAM modules if necessary.

DRAM Removal

If it is necessary to remove SO-DIMM DRAM modules, perform the steps below. Review the topic "DRAM Installation and Removal Overview" before removing the DRAM modules.

1. Put on an anti-static grounding strap.
2. Make sure the system is turned off.
3. Remove the ZT 8908 from the card cage.

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4. The left and right ejectors of the DRAM socket are flexible to assist removal and installation of DRAM modules. Modules are removed by freeing them from the left and right ejectors one at a time. Using your fingers, grasp the edges of the top DRAM module and lift gently, applying outward pressure on the left ejector until the left side of the module is free from the socket.

5. Continue to gently lift the DRAM module, applying outward pressure on the right ejector until the right side of the module is free from the socket.

6. Grasp the bottom edge of the DRAM module with your fingers and pull it toward the socket's open end. The DRAM module should come out easily.

7. Repeat steps 4 - 6 for the bottom DRAM module.

DRAM Installation

If it is necessary to install SO-DIMM DRAM modules, perform the steps below. Review the topic "DRAM Installation and Removal Overview" before installing DRAM modules.

1. Put on an anti-static grounding strap.

2. Make sure the system is turned off.

3 Remove the ZT 8908 from the card cage.

4. The socket's right ejector is keyed to accommodate the notched end of the DRAM module, thereby preventing incorrect installation of the module. Install the notched end of the bottom DRAM module into the keyed ejector by gently pushing the module into the socket. If the DRAM module goes in crooked, it is probably in backwards.

5. Gently push down on the DRAM module until it latches into place. If it seems that too much pressure is required, use your fingers to gently push the ejectors outward until the DRAM module is seated in the socket.

6. Repeat Steps 4 - 6 to install the top DRAM module.

BIOS SETUP OVERVIEW

The ZT 8908 has many features configurable through the BIOS Setup utility. The Setup utility is executed during the boot sequence when the **"s"** key is typed. In DOS systems, Setup may be executed by running the SETUP.COM program from the command line.

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BIOS SETUP Screens

The BIOS Setup utility for the ZT 8908 is organized as two screens, listed below.[†]

- Screen 1: **Generic option list.** Options shared among all Ziatech CPUs are listed on this screen. Base memory and extended memory size selection, boot source, hard disk type, and floppy disk type are configurable through this screen.
- Screen 2: **ZT 8908-specific SETUP options.** Options such as interrupt routing and STD 32 memory and I/O addressing are configurable through this screen. See the following topic, "ZT 8908-Specific Setup Options," for more information.

The parameters in the Setup screens are easily changed. Use the arrow keys to select a parameter, then press **+** or **-** to step through the valid choices for that parameter. A dynamic help line at the bottom of the screens helps you determine how to set each parameter. Setup accepts only valid parameter sets: if changing one parameter invalidates another, Setup automatically updates the invalid parameter. After setting the parameters, press the F10 key to accept them. Press the **Page Down** and **Page Up** keys to switch between Setup screens.

ZT 8908-Specific SETUP Options

ZT 8908-specific Setup options, such as interrupt routing and STD 32 memory addressing, are configurable through Screen 2 of the BIOS Setup utility and are discussed below.

- Interrupt routing

  The source for individual interrupt controller inputs is selectable through the Setup utility. The STD 32 backplane interrupts, frontplane interrupts, and PCI interrupts are options.

- Backplane DMA (via BUSRQ*/BUSAK*) channel selection

  Normally, the BUSRQ*/BUSAK* signals are used to allow DMA to a backplane-based floppy disk controller (for example, ZT 8954), but other devices may use this mechanism in the absence of a floppy disk controller. The channel is selectable between channel 2 (for floppy disks) and channel 5 (for 16-bit operations).

[†] A third screen is used for STAR SYSTEM configuration options on permanent master CPUs. Refer to the STD 32 STAR SYSTEM User's Manual for more information.

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- STD 32 memory address decoding

  Locations in the lower 1 Mbyte and in extended memory can be dedicated to the STD 32 bus. Regions that are configured for STD 32 cannot be used for PCI peripherals. The following regions are selectable:

  † 000C8000h - 000CFFFFh (This region must be set to STD 32 for STAR SYSTEM operation)
  † 000D0000h - 000D7FFFh
  † 000D8000h - 000DFFFFh

DIP SWITCH SETTINGS AND LOCATIONS

The ZT 8908 includes three banks of switches. The "Factory Default DIP Switch Configuration" figure illustrates the factory default switch settings for ZT 8908 boards purchased in a DOS system. The "Customer DIP Switch Configuration" illustration provides a blank switch layout; use this figure to document your switch configuration if it differs from the factory default.

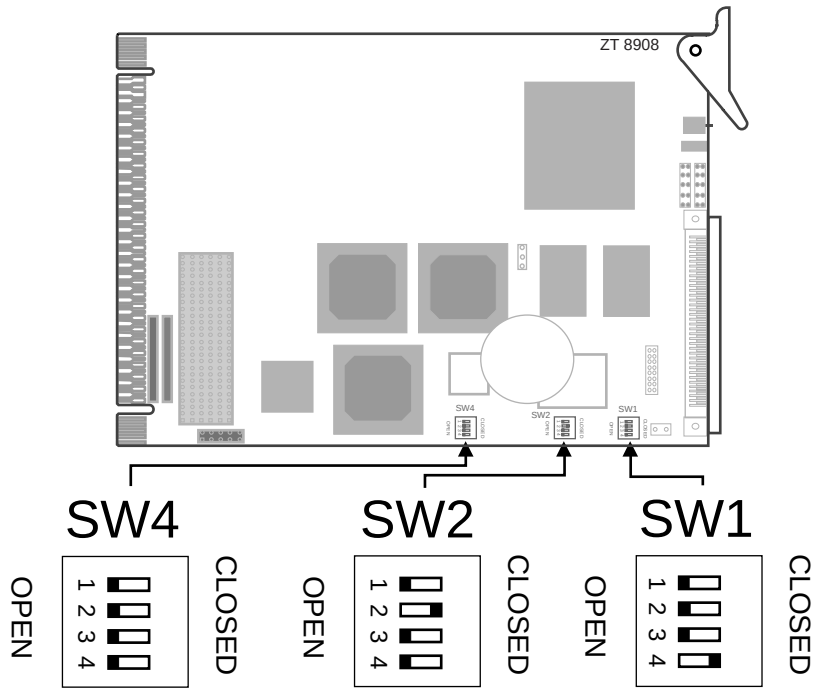
The "DIP Switch Cross Reference" table below lists each switch and its function.

DIP Switch Cross Reference

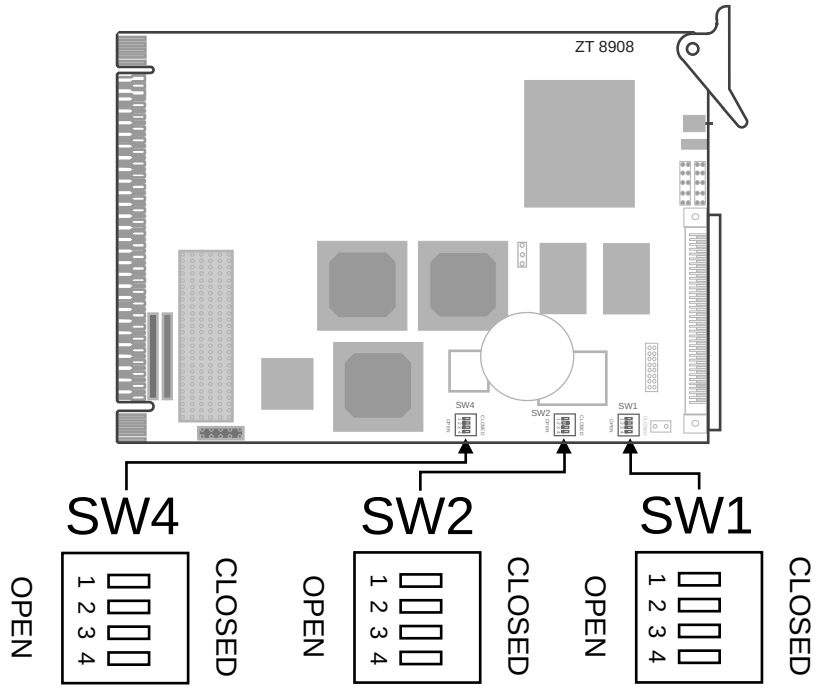
Function	Switches
CMOS RAM Battery Back Up	SW2-2
CMOS RAM Erase	SW2-3
Flash Write Protect	SW2-1
BIOS Recovery Device Enable	SW1-3
EA/SA Transfer Enable	SW1-4
Port 80h Snoop Enable	SW2-4
Software ID Inputs 0-3	SW4-1 to SW4-4
Spare (***must be left open***)	SW1-2
Video Emulation SRAM Enable	SW1-1

† Indicates default decoding

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Factory Default DIP Switch Configuration



Customer DIP Switch Configuration

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DIP SWITCH DESCRIPTIONS

The following topics list the DIP switches in numerical order and provide a detailed description of each switch. A dagger (†) indicates the default DIP switch configuration.

Note that where switches are referenced in this chapter, "SWx" corresponds to the DIP switch number and "-N" corresponds to the DIP switch position (for example, SW2-3 means "DIP switch bank 2, position 3"). A switch referred to as "closed" can also be said to be "on."

SW1-1 (Video Emulation SRAM Enable)

SW1-1 enables/disables the Video Emulation SRAM (128K x 8 SRAM) in socket U14. By default (SW1-1 = Open), video emulation is disabled. To enable the SRAM in socket U14 for video emulation, close SW1-1.

See the topic, "STAR SYSTEM Video Emulation SRAM," in Chapter 16 for step-by-step instructions.

	SW1 - 1	Function
†	Open	Disable Video Emulation SRAM
	Closed	Enable Video Emulation SRAM

SW1-2 (Spare Switch)

This switch is reserved for use by Ziatech and must be left open. ***Closing this switch will damage the board.***

SW1-3 (BIOS Recovery Device Enable)

SW1-3 enables/disables the BIOS Recovery Device (ZT 95207) in socket U14. By default, the BIOS Recovery Device is disabled. To enable the BIOS Recovery Device, set SW1-3 to the closed position.

See "BIOS Recovery" in Chapter 16 for step-by-step instructions.

	SW1 - 3	Function
†	Open	Disable BIOS Recovery Device
	Closed	Enable BIOS Recovery Device

† Factory default configuration

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SW1-4 (EA/SA Transfer Enable)

SW1-4 enables either EA/SA (default), or SA-only backplane transfers. If none of your peripheral boards are extended architecture, selecting SA-only (SW1-4 = Open) provides improved backplane performance.

	SW1 - 4	Function
	Open	SA-only backplane transfers
†	Closed	EA/SA backplane transfers

SW2-1 (Flash Write Protect)

SW2-1 enables/disables write protection for the BIOS and flash memory. When SW2-1 is open (default), the flash is writable. When SW2-1 is closed, the flash is write protected, preventing software from changing the contents of flash memory.

Note: SW2-1 must be open when using the FLASH.EXE utility to recover a corrupted BIOS.

	SW2 - 1	Function
†	Open	Disable flash write protect
	Closed	Enable flash write protect

SW2-2, SW2-3 (CMOS Clear / Battery Backup)

These switches are used to battery-back and clear the CMOS memory. When closed (default), SW2-2 connects the CMOS memory to the on-board battery. For normal operation this switch should remain in the closed position. If for some reason the CMOS needs to be cleared, perform the following steps:

1. Power off the system and remove the ZT 8908 from the card cage.
2. Open SW2-2 and close SW2-3.
3. Close SW2-2 and open SW2-3.
4. Reinstall the ZT 8908 into the card cage and reboot the system. The CMOS is restored to its factory default settings.

Note: Do not have SW2-2 and SW2-3 closed at the same time. Doing so will drain the on-board battery.

---

† Factory default configuration

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	SW2-2	SW2-3	CMOS Configuration RAM
	Open	Closed	Clear CMOS (return to default after clearing)
†	Closed	Open	Normal operation - CMOS battery-backed

SW2-4 (Port 80h Snoop Enable)

SW2-4 is used mainly for diagnostic purposes and software debugging. Closing SW2-4 allows I/O writes to Port 80h to be passed to the STD 32 Bus.

	SW2-4	Function
	Closed	Enable Port 80h snooping
†	Open	Disable Port 80h snooping

SW4-1 - SW4-4 (Software ID Inputs 0-3)

Switches SW4-1 through SW4-4 are configurable as general purpose inputs for software revision control, configuration setup, or other user-defined options. These bits are accessed by the Intel 430TX PCIset as shown in the table below. By default, all positions on bank SW4 are open.

Note: Ziatech may define these bits in the future.

Switch	Default Position	Function
SW4-1	Open	PIIX4 General Input 13
SW4-2	Open	PIIX4 General Input 14
SW4-3	Open	PIIX4 General Input 15
SW4-4	Open	PIIX4 General Input 16

RESISTOR PACK OPTIONS

In a multiple master architecture, one processor board must be configured as a permanent master. The remaining processor boards must be configured for temporary

† Factory default configuration

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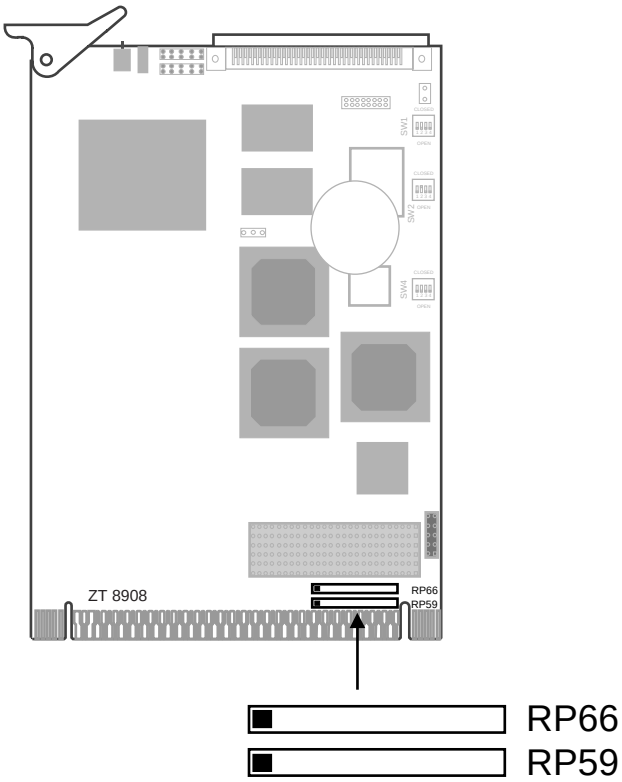
master operation. The permanent master is responsible for managing the STD bus clock, CLOCK* (P49), and the system reset, SYSRESET* (P47).

Installing resistor packs RP59 and RP66 (default) configures the ZT 8908 as a permanent master; removing RP59 and RP66 configures the ZT 8908 as a temporary master. RP59 and RP66 are located near the ZT 8908's gold STD 32 P/E backplane connector, as shown in the "Resistor Pack Locations" illustration.

RP59 and RP66 also provide pullup resistors for the SA open collector signals on the STD 32 backplane. As there can only be one master that provides the pullup mechanism, it is logical to always have the permanent master perform this function.

RP59 and RP66	ZT 8908 Implementation	STD 32 Bus Signals
Installed	Permanent Master in a STAR SYSTEM or Single Master in a non-STAR SYSTEM	Pulled up; CLOCK* and SYSRESET* driven by this CPU
Installed	ZT 8908 is operating as a stand-alone processor not installed in a backplane	———
Removed	Temporary Master in a STAR SYSTEM or stand-alone processor in a backplane with other CPUs	Not pulled up; CLOCK* and SYSRESET* not driven by this CPU

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Resistor Pack Locations

CUTTABLE TRACE OPTIONS AND LOCATIONS

The ZT 8908 contains several cuttable traces (zero Ω shorting resistors) that allow the user to configure other board options. The "Cuttable Trace Locations" figure shows the placement of the ZT 8908 cuttable traces. The "Cuttable Trace Definitions" table provides a quick cross-reference for the ZT 8908 cuttable trace descriptions that follow.

There are two types of cuttable traces on the ZT 8908: single-option and double-option. **Single option** cuttable traces (labeled CT**x--**for example, CT2) have two surface mount pads. A zero ohm shorting resistor is then soldered between these pads to make the connection. **Double option** cuttable traces (labeled CT**x** "A" and "B" — for example, CT1A and CT1B) are implemented using three surface mount pads. The zero ohm shorting resistor is then soldered between one set of pads, depending on the chosen option.

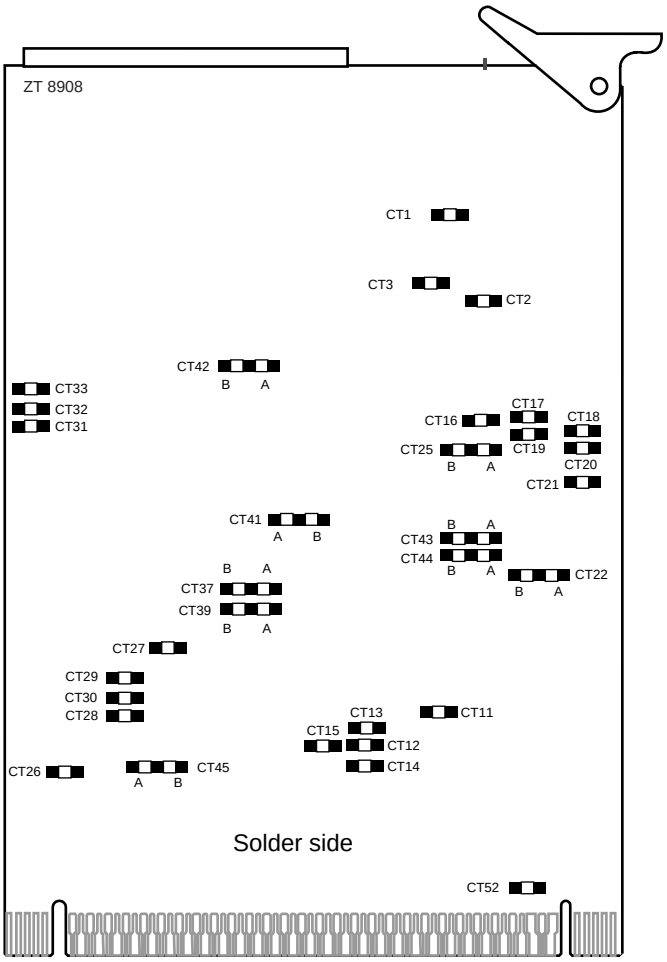
Note: Cuttable trace modifications should only be performed by a qualified technician familiar with surface mount soldering techniques. The product warranty is voided if the board is damaged by customer modifications. If a qualified technician is not available to you, contact Ziatech Technical Support. For large production orders Ziatech can also set up specials that are pre-configured at the factory. Contact Ziatech for more information.

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Cuttable Trace Definitions

CT#	DEFAULT	DESCRIPTION
CT1	—	CPU Speed Multiplier Settings
CT2	—	CPU Speed Multiplier Settings
CT3	—	CPU Speed Multiplier Settings
CT11	In	CPU Interface Voltage Select (3.3 V)
CT12	Out	CPU Interface Voltage Select (3.3 V)
CT13	In	CPU Interface Voltage Select (3.3V)
CT14	In	CPU Interface Voltage Select (3.3 V)
CT15	Out	CPU Interface Voltage Select (3.3 V)
CT16	In	DC – DC Share Circuitry
CT17	—	CPU Interface Voltage Select (2.8 V)
CT18	—	CPU Interface Voltage Select (2.8 V)
CT19	—	CPU Interface Voltage Select (2.8 V)
CT20	—	CPU Interface Voltage Select (2.8 V)
CT21	—	CPU Interface Voltage Select (2.8 V)
CT22	A	STAR SYSTEM Interrupt Select (INTRQ4*)
CT25	B	Fan Voltage 5 V/12 V (12 V default)
CT26	In	Board Revision ID
CT27	In	Board Revision ID
CT28	In	Board Revision ID
CT29	In	Board Revision ID
CT30	In	Board Revision ID
CT31	Out	CPU Frequency Select
CT32	Out	CPU Frequency Select
CT33	In	CPU Freq. Select
CT37	B	DRQ1 Select
CT39	A	DACK0/DACK5 Select
CT41	A	DACK1/DACK6 Select
CT42	B	DRQ3 Select
CT43	A	DACK3 Select
CT44	A	DACK7 Select
CT45	B	IRQ15 Select
CT52	In	INTRQ4* STD Connection

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Cuttable Trace Locations

CT1 - CT3 (CPU Speed Multiplier Settings)

CT1, CT2, and CT3 are used to set the multiplication factor of the internal CPU clock. These cuttable traces are set at the factory and should not be changed by the user. Since not all processors support all the settings shown in the table below, the ZT 8908 may not operate if these cuttable traces are changed.

CPU Speed (MHz)	Core Multiplier	CT1 (BF2)	CT2 (BF1)	CT3 (BF0)
133 MHz	2.0x	Out	Out	In
	2.5x	Out	In	In
233 MHz	3.5x	Out	Out	Out
266 MHz	4.0x	In	Out	In

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CT11-CT15, CT17-CT21 (CPU Interface Voltage Select)

These cuttable traces set the CPU I/O (CT11-CT15) and CPU core (CT17-CT21) voltages. These cuttable traces are set at the factory and should not be changed by the user. Doing so may damage the processor.

CT11/CT17	CT12/CT18	CT13/CT19	CT14/CT20	CT15/CT21	Voltage
Out	Out	Out	Out	Out	1.244
Out	Out	Out	Out	In	1.340
In	Out	Out	Out	In	1.390
Out	In	Out	Out	In	1.440
In	In	Out	Out	In	1.490
Out	Out	In	Out	In	1.540
In	Out	In	Out	In	1.590
Out	In	In	Out	In	1.640
In	In	In	Out	In	1.690
Out	Out	Out	In	In	1.740
In	Out	Out	In	In	1.790
Out	In	Out	In	In	1.840
In	In	Out	In	In	1.890
Out	Out	In	In	In	1.940
In	Out	In	In	In	1.990
Out	In	In	In	In	2.040
In	In	In	In	In	2.090
In	Out	Out	Out	Out	2.140
Out	In	Out	Out	Out	2.240
In	In	Out	Out	Out	2.340
Out	Out	In	Out	Out	2.440
In	Out	In	Out	Out	2.540
Out	In	In	Out	Out	2.640
In	In	In	Out	Out	2.740
Out	Out	Out	In	Out	2.840
In	Out	Out	In	Out	2.940
Out	In	Out	In	Out	3.040
In	In	Out	In	Out	3.140
Out	Out	In	In	Out	3.240
‡ In	‡ Out	‡ In	‡ In	‡ Out	3.340
Out	In	In	In	Out	3.440
In	In	In	In	Out	3.540

Note: The CPU I/O voltage is set to 3.3 V by default. The CPU core voltage will vary depending on the type of CPU installed.

‡ CT11-CT15 (CPU I/O Voltage) factory default configuration

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CT16 (DC-DC Share Circuitry)

Configuration of CT16 enables/disables the DC-DC shared circuitry. This function is disabled by default (CT16 = Out). Enabling DC-DC shared circuitry balances the load on the 3.3 V DC-to-DC converters and should only be enabled if both the CPU I/O and core voltages are the same and are shorted together through the CPU (see the previous topic "CPU Interface Voltage Select").

	CT16	Function
†	Out	Disable DC-DC Sharing Circuitry
	In	Enable DC-DC Sharing Circuitry

CT22 (STAR SYSTEM INTRQ4* Select)

Configuration of CT22 connects the STAR interrupt to INTRQ* or INTRQ4* (default).

	CT22	Function
†	A	STAR interrupt connected to INTRQ4*
	B	STAR interrupt connected to INTRQ*

CT25 (Fan Voltage Select)

CT25 selects the voltage for the processor cooling fan.

Position	Fan Voltage
A	5 V
† B	12 V

CT26-CT30 (Board Revision)

These cuttable traces are set at the factory depending on the current board revision and should not be modified by the user.

† Factory default configuration

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CT31-CT33 (Bus Frequency Select)

CT31, CT32, and CT33 are used to control the CPU/PCI bus frequency. The PCI bus frequency is always one-half of the CPU bus frequency. The CPU speed multiplier is set by CT1-CT3.

	Speed (MHz)		Cuttable Traces		
	CPU Frequency	PCI Frequency	CT31	CT32	CT33
	50	25	Out	In	In
	60	30	Out	In	Out
†	66.6	33.3	Out	Out	In

CT37, CT39, CT41-CT44 (Frontplane DMA Channel Select)

The ZT 8908 supports either 8-bit or 16-bit frontplane DMA, available on connector J7. Up to four frontplane DMA channels are available simultaneously. These cuttable traces configure the four chosen frontplane DMA channels to be either 8-bit or 16-bit. Be sure to mask unused channels not required by the application. See Chapter 6, "DMA Controller," for more information.

Default Frontplane DMA Settings

	Channel Selection	Cuttable Trace	Data Size	Available on J7...
†	DMA channel 0	CT39B	8-bit	pins 1 (DRQ) and 3 (DACK)
†	DMA channel 1	CT41B, CT37B	8-bit	pins 2 (DRQ) and 4 (DACK)
†	DMA channel 7	CT42B, CT43A, CT44A	16-bit	pins 5 (DRQ) and 7 (DACK)

Alternate Frontplane DMA Settings

	Channel Selection	Cuttable Trace	Data Size	Available on J7...
	DMA channel 5	CT39A	16-bit	pins 1 (DRQ) and 3 (DACK)
	DMA channel 6	CT41A, CT37B	16-bit	pins 2 (DRQ) and 4 (DACK)
‡	DMA channel 3	CT42A, CT43B, CT44B	8-bit	pins 5 (DRQ) and 7 (DACK)

† Factory default configuration

‡ By default, DMA channel 3 is assigned to the on-board parallel printer port (for ECP operation). Route DMA channel 3 to connector J7 by configuring CT42, CT43, and CT44 as shown above.

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CT45 (IRQ15 Input Source Selection)

Configuration of CT45 routes the sources described below to the interrupt controller IRQ15 input.

Connector J5, pin E4: When CT45A is installed, IRQ15 is connected to J5 (PCI Mezzanine Local Bus Interface Connector), pin E4 (secondary IDE interrupt signal INTS).

Connector J6, pin 8: When CT45B is installed (default), IRQ15 is connected to J6 (Frontplane Interrupt Connector), pin 8. This configuration is typically used when connecting a secondary IDE controller, such as the ZT 8944.

	CT45	Source Routed to Interrupt Controller IRQ15 Input
	A	Connector J5, pin E4 (INTS = secondary IDE interrupt)
†	B	Connector J6, pin 8 (FP6*)

CT52 (INTRQ4* STD Connection)

Configuration of CT52 selects the function of pin P5 on the STD 32 connector. By default (CT52 = In), the ZT 8908 uses pin P5 for signal INTRQ4*. However, some STD 32 systems define P5 for VBAT (battery backup). If the ZT 8908 is used in a system that requires P5 to be configured as VBAT, then CT52 should be removed.

	CT52	Function
†	In	STD 32 connector pin P5 for INTRQ4*
	Out	STD 32 connector pin P5 for VBAT

Note: Do not remove CT52 if resistors RP59 and RP66 are also removed, as when the ZT 8908 is configured as a STAR SYSTEM temporary master. If you need to operate the ZT 8908 in this configuration (VBAT operation with RP59 and RP66 removed), contact Ziatech for assistance.

† Factory default configuration

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B. SPECIFICATIONS

This appendix describes the following specifications:

- Electrical and environmental specifications of the ZT 8908.
- Mechanical specifications of the ZT 8908.

This appendix also includes illustrations of the board dimensions, the P/E connector pinouts, as well as tables showing the pin assignments for the ZT 8908's 11 connectors.

ELECTRICAL AND ENVIRONMENTAL

This section covers the following electrical and environmental specifications.

- Absolute maximum ratings
- DC operating characteristics
- Battery backup characteristics
- STD bus loading characteristics

Absolute Maximum Ratings

Supply Voltage, Vcc:	4.75 to 5.25 V
Supply Voltage, +12 V:	11.4 to 12.6 V
Storage Temperature:	-40º to +85º Celsius
Operating Temperature:	0º to +70º Celsius
Non-Condensing Relative Humidity:	<95% at 40º Celsius

Operating Temperature

The values in the figures and tables referenced below are stress ratings only. Do not operate the ZT 8908 at these maximums. See the "DC Operating Characteristics" section in this appendix for operating conditions.

For proper operation, the ZT 8908 case temperature must remain below 70º C for both the AMD-K6 and Pentium processors. Contact Ziatech for *Ambient Temperature Vs. AMD-K6 Processor (MMX) Case Temperature* information. An integrated fan/heatsink is provided with the processors to help maintain these requirements.

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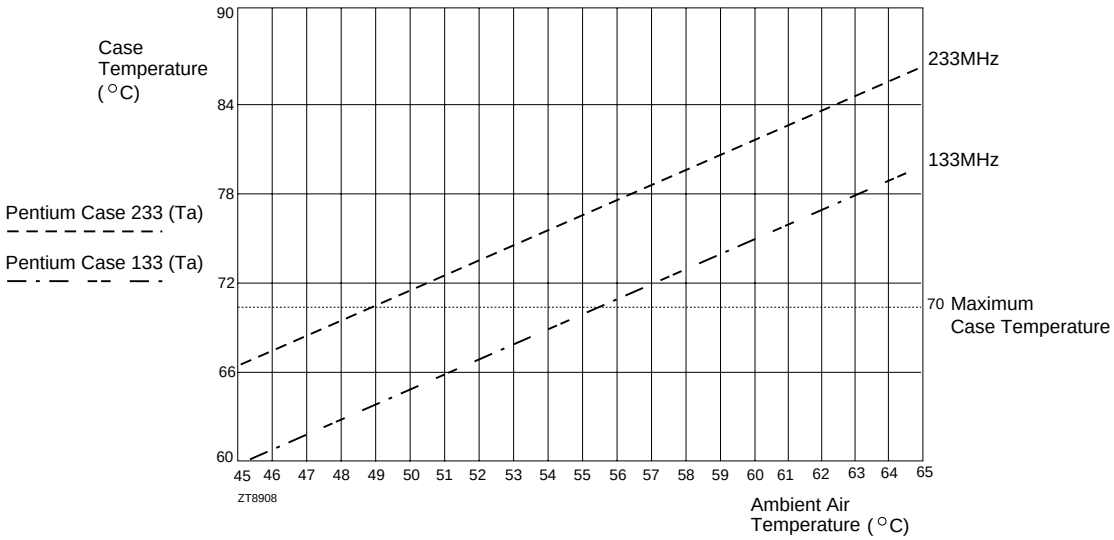
- "Ambient Temperature Vs. Pentium Processor Case Temperature" figure.
- "AMD-K6 Processor Maximum Ambient Temperature" table.
- "Pentium Processor Maximum Ambient Temperature" table.

Pentium Processor Maximum Ambient Temperature

Processor Speed (MHz)	Max. Ambient Temperature (°C)
133	56
233 (MMX)	49

AMD-K6 Processor Maximum Ambient Temperature

Processor Speed (MHz)	Max. Ambient Temperature (°C)
266	50



Ambient Temperature Vs. Pentium Processor Case Temperature (With Heatsink)

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DC Operating Characteristics

- Supply Voltage, Vcc: 4.75 to 5.25 V
- Supply Voltage, AUX +: 11.4 to 12.6 V
- Supply Voltage, AUX -: Not used
- Supply Current, Icc:

  P54C Pentium Processors

  – Pentium-133: 3.3 A typ., 3.7 A max.

  P55C (MMX) Pentium Processors

  – Pentium-233: 4.5 A typical, 5.0 A max.

  AMD K6 (MMX) Processors

  – AMD K6-266: 3.8 A typical, 4.0 A max.

  (Numbers assume 32 Mbytes of DRAM and 2 Mbytes of flash, no video option)

  64 Mbytes of DRAM add 50 mA

  128 Mbytes of DRAM add 100 mA
- Supply Current, AUX + (12 V):

  – 8 Mbyte flash option: 0.020 A typ., 0.030 A max.

  – Fan/Heatsink: 120 mA typ., 200 mA max.

Battery Backup Characteristics

Battery Backup Battery Voltage:	3 V
Battery Capacity:	255 mAH
Real-time clock requirements:	5 µA max.[†]
Electrochemical Construction:	Poly-carbonmonofluoride

[†] When Vcc is below acceptable operating limits

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STD-80 Compatibility

The ZT 8908 is designed for use in an STD 32 backplane environment. While designed to be backward compatible with STD-80 systems, the ZT 8908 is not guaranteed to work in all system topologies.

STD Bus Loading Characteristics

The unit load is a convenient method for specifying the input and output drive capability of STD bus cards. With this method, one unit load is equal to one LSTTL load as follows:

- Current for single input load: 20 µA
- Current for single output drive: -400 µA

The unit load reflects current requirements at worst case conditions over the recommended supply voltage and operating temperature ranges. An output drive of 60 unit loads drives 60 STD bus cards having input ratings of one unit load. The table "STD Bus Loading, P Connector" includes load values for STD-80 connections. The table "STD Bus Loading, E Connector" includes load values for STD 32 connections.

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STD Bus Loading, P Connector

PIN (CIRCUIT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC							PIN (COMPONENT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC
+5 VDC	REQ		P2	P1		REQ	+5 VDC
GND	REQ		P4	P3		REQ	GND
DCPDN*		40	P6	P5	24	1	INTRQ4* (VBAT)
D7/A13 [1]	1	24	P8	P7	24	1	D3/A19 [1]
D6/A22 [1]	1	24	P10	P9	24	1	D2/A18 [1]
D5/A21 [1]	1	24	P12	P11	24	1	D1/A17 [1]
D4/A20 [1]	1	24	P14	P13	24	1	D0/A16 [1]
A15	1	24	P16	P15	24	1	A7
A14	1	24	P18	P17	24	1	A6
A13	1	24	P20	P19	24	1	A5
A12	1	24	P22	P21	24	1	A4
A11	1	24	P24	P23	24	1	A3
A10	1	24	P26	P25	24	1	A2
A9	1	24	P28	P27	24	1	A1
A8	1	24	P30	P29	24	1	A0
RD*	1	24	P32	P31	24	1	WR*
MEMRQ*	1	24	P34	P33	24	1	IORQ*
BHE	1	24	P36	P35	24	1	IOEXP
ALE*	1	24	P38	P37		1	INTRQ1*
STATUS 0*	1	24	P40	P39	24	1	STATUS 1*
BUSRQ* [2]	1	24	P42	P41	24	1	BUSAK* [2]
INTRQ*	1	24	P44	P43			INTAK*
NMIRQ*	1		P46	P45		1	WAITRQ*
PBRESET*	1		P48	P47	24	1	SYSRESET* [3]
INTRQ2* (CNTRL*)	1		P50	P49	24	1	CLOCK* [3]
PCI [4]	1		P52	P51			PCO [4]
AUX GND	REQ		P54	P53		REQ	AUX GND
AUX-V			P56	P55		REQ	AUX+V

ZT8908

Notes:

REQ indicates required connection.

[1] High order address bits multiplied over the data bus.

[2] BUSRQ* and BUSAK* are bi-directional

[3] SYSRESET* and CLOCK* are outputs in permanent master configuration and inputs in temporary master configuration.

[4] PCI is connected to PCO.

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STD Bus Loading, E Connector

PIN (CIRCUIT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC							PIN (COMPONENT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC
RSVD			E2	E1			GND
XA23	1	24	E4	E3	24	1	XA19
XA22	1	24	E6	E5	24	1	XA18
XA21	1	24	E8	E7	24	1	XA17
XA20	1	24	E10	E9	24	1	XA16
RSVD			E12	E11			NOWS*
+5 VDC	REQ		E14	E13		REQ	+5 VDC
DREQx*		24	E16	E15		1	DAKx*
GND	REQ		E18	E17		REQ	GND
D31	1	24	E20	E19	24	1	D27
D30	1	24	E22	E21	24	1	D26
D29	1	24	E24	E23	24	1	D25
D28	1	24	E26	E25	24	1	D24
GND	REQ		E28	E27	24	1	D23
D15	1	24	E30	E29	24	1	D22
D14	1	24	E32	E31	24	1	D21
D13	1	24	E34	E33	24	1	D20
D12	1	24	E36	E35		REQ	GND
D11	1	24	E38	E37	24	1	D19
D10	1	24	E40	E39	24	1	D18
D9	1	24	E42	E41	24	1	D17
D8	1	24	E44	E43	24	1	D16
MASTER16*	1	24	E46	E45		REQ	GND
AENx*			E48	E47			IRQx
BE3*	1	24	E50	E49	24	1	BE1*
BE2*	1	24	E52	E51	24	1	BE0*
GND	REQ		E54	E53	24	1	MEM16*
W-R	1	24	E56	E55	24	1	M-IO
DMAIOR*		24	E58	E57	24	1	DMAIOW*
EX8*	1		E60	E59		1	IO16*
START*		24	E62	E61	24	1	CMD*
EX32*	1		E64	E63		1	EX16*
T-C		24	E66	E65		1	EXRDY
+5 VDC	REQ		E68	E67		1	INTRQ3*
MREQx*		24	E70	E69		1	MAKx*
MSBURST*		24	E72	E71		1	SLBURST*
XA31*	1	24	E74	E73	24	1	XA27*
XA30*	1	24	E76	E75	24	1	XA26*
XA29*	1	24	E78	E77	24	1	XA25*
XA28*	1	24	E80	E79	24	1	XA24*

Note: REQ indicates required connection.

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RELIABILITY

MTBF: 95,996 hrs (11 years)

MTTR: 5 minutes (based on board replacement)

MECHANICAL

This section covers the following mechanical specifications:

- Card dimensions and weight
- Connectors (including connector locations, descriptions, and pinouts)
- Cables

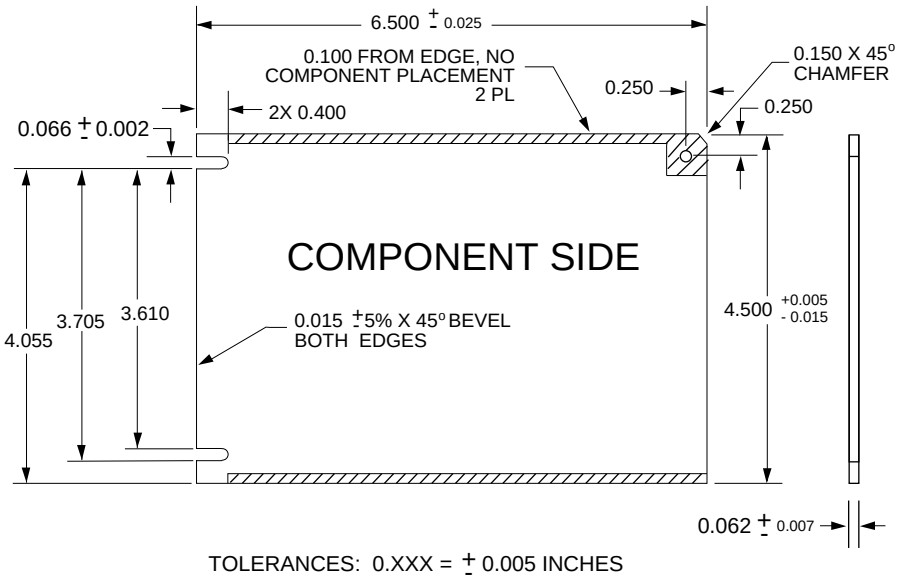
Board Dimensions and Weight

The ZT 8908 meets the *STD-32 Series Bus Specification* for all mechanical parameters. In a card cage with 0.625 inch spacing, the ZT 8908 requires two card slots with or without the PCI Mezzanine adapter installed. The "Board Dimensions" figure following shows the mechanical dimensions of the ZT 8908.

Length:	16.51 ± 0.063 cm (6.500 ± 0.025 inches)
Width:	11.43 ± 0.038 cm (4.500 ± 0.015 inches)
Thickness:	0.158 ± 0.013 cm (0.062 ± 0.005 inches)
Weight:	288.16 grams (10.2 ounces)†
Height From Top Surface:	1.27 cm (0.5 inches)
Height From Bottom Surface:	0.11 cm (0.043 inches)

† With video card, fan/heatsink, and 32 Mbytes of DRAM

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Board Dimensions

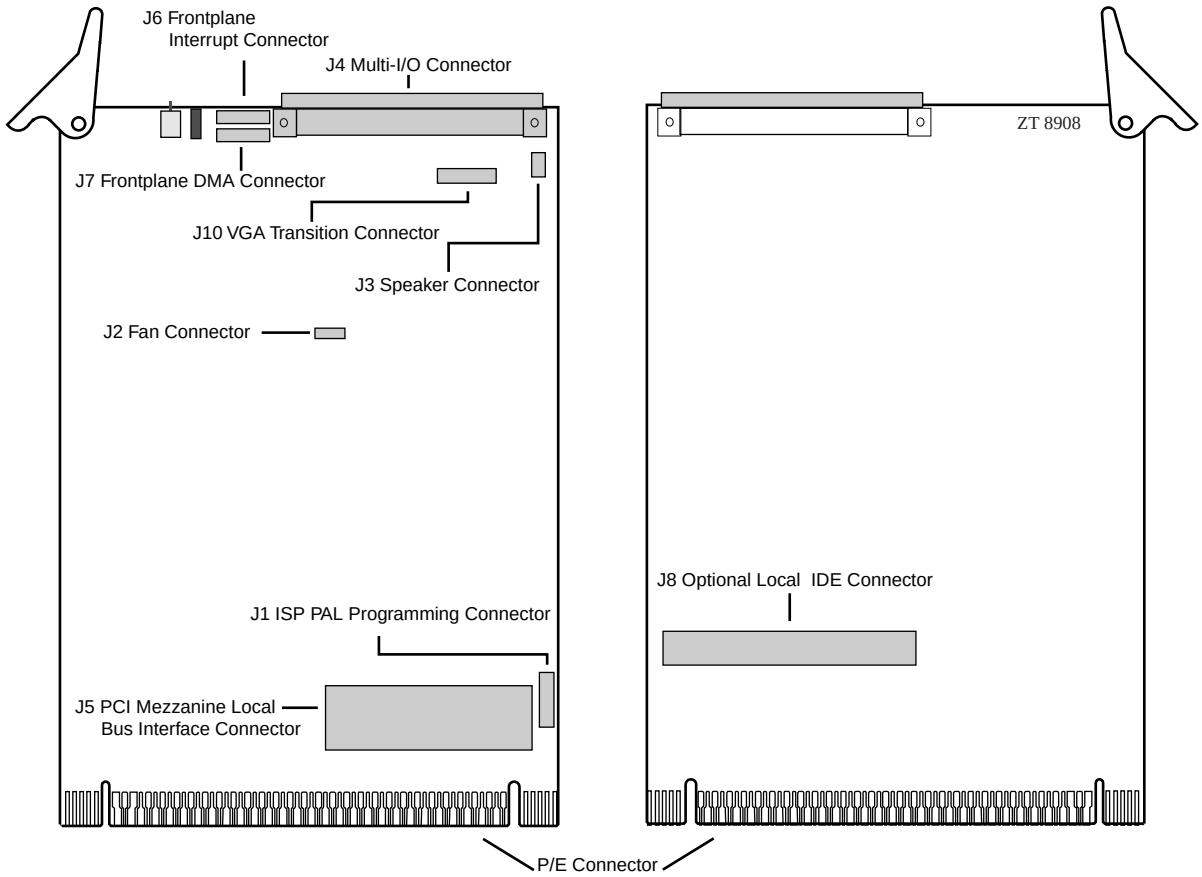
Connectors

As shown in the "Connector Locations" illustration, the ZT 8908 includes several connectors to interface to the STD bus and application-specific devices. A brief description of each connector is shown in the "Connector Assignments" table. A complete description and pinout for each connector is provided in the following topics.

Connector Assignments

Connector	Function
J1	ISP PAL™ Programming Connector
J2	Fan Connector
J3	Speaker Connector
J4	Multi-I/O Connector
J5	PCI Mezzanine Local Bus Interface Connector
J6	Frontplane Interrupt Connector
J7	Frontplane DMA Connector
J8	Optional IDE Connector
J10	VGA Transition Connector

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Connector Locations

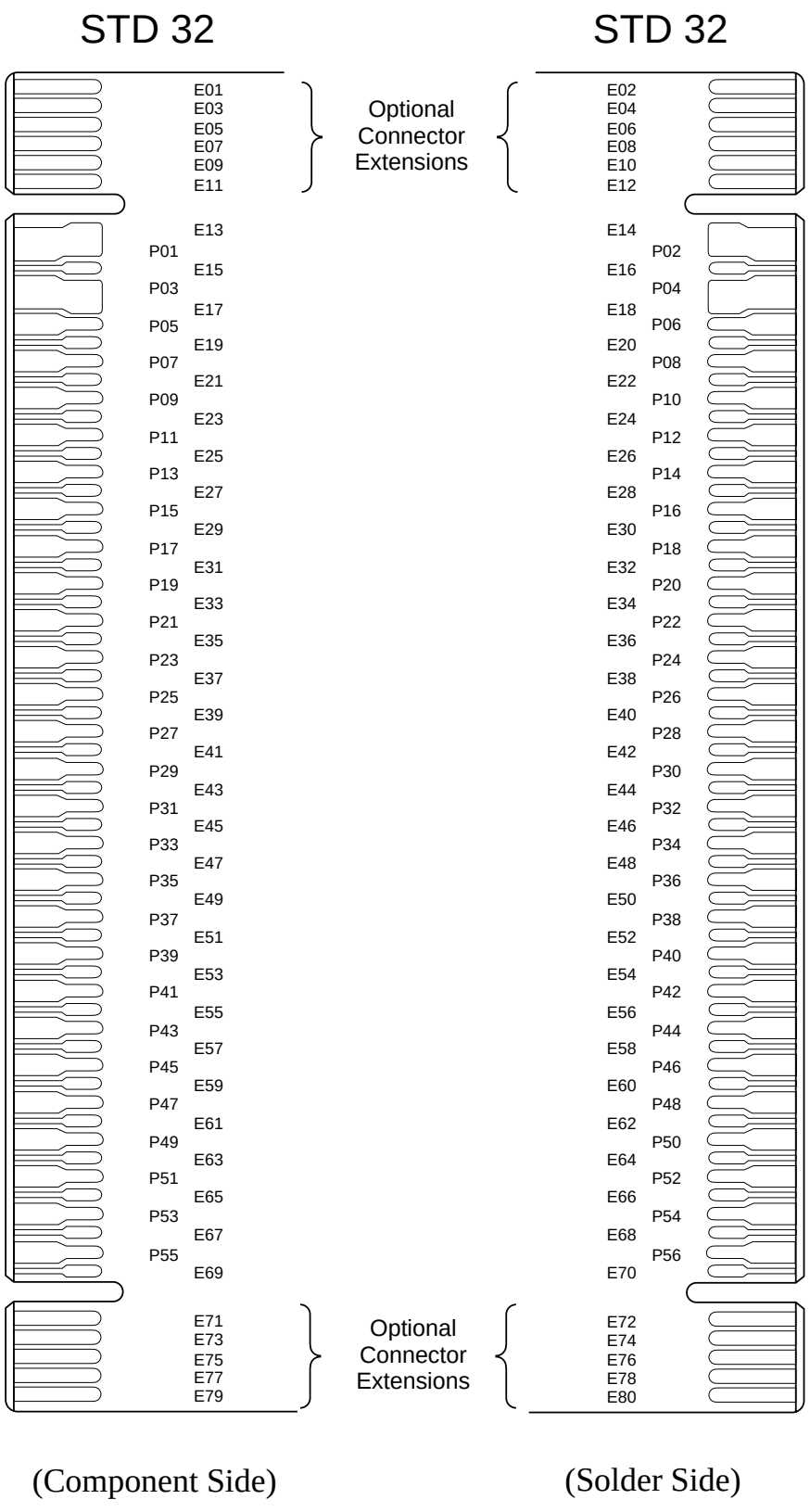
STD 32 P/E Connector

P: The P connector is the interface between the ZT 8908 and the STD-80 bus. This connector is a 56-pin (dual 28-pin) card-edge connector with fingers on 0.125 inch contact spacing. The mating connector is a Viking 3VH28/1CNK5 or equivalent for the solder tail, or a Viking 3VH28/1CND5 or equivalent for a three-level wire wrap.

E: The E connector extends the P connector to interface the ZT 8908 to the STD 32 bus. This connector combines with the P connector to make a 114-pin (dual 57-pin) card-edge connector with fingers on 0.0625 inch contact spacing. The mating connector is a Viking S3VT68/5DP12 or equivalent for the solder tail, or a Viking S3VT68/5DE12 or equivalent for the card extender.

Pinouts: The "P/E Connector Pinout" illustration shows pin assignments for the P and E connectors. See the "STD Bus Loading, P Connector" and the "STD Bus Loading, E Connector" table for signal assignments.

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P/E Connector Pinout

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J1 (ISP PAL™ Programming Connector)

J1, a 2 x 5 2 mm header, is the In-System Programming connector used during the manufacturing process to program the on-board ISP logic. No user function exists. The pin assignments are given in the "J1 (ISP PAL Programming Connector) Pinout" table.

J1 (ISP PAL Programming Connector) Pinout

Pin #	Signal	Pin #	Signal
1	GND	2	SDO
3	GND	4	SDI
5	GND	6	SCLK
7	GND	8	MODE
9	VCC	10	ISPEN

J2 (Fan Connector)

J2 is a 3-pin vertical male header with 0.1 inch contact spacing for supplying power to the fan/heatsink. Select +12 VDC or +5 VDC configuration with cuttable trace CT25. Pin 3 is an optional tachometer input from fans so equipped. The pin assignments are given in the "J2 (Fan Connector) Pinout" table. The mating connector is a Molex 39-01-0023 or equivalent. The mating connector also requires two Molex 39-01-0031 terminals or equivalent.

J2 (Fan Connector) Pinout

Pin #	Signal	Type	Description
1	PWR	Out	+12V or (+5V) depending on CT25
2	GND	—	Ground
3	FANOUT	—	Tach output if supported by fan

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J3 (Speaker Connector)

J3 is a latching 2-pin male low-profile header with 0.1 inch contact spacing. The speaker signals are available through this connector. The pin assignments are given in the "J3 (Speaker Connector) Pinout" table. The mating connector is a Molex 39-01-0023 or equivalent. The mating connector also requires two Molex 39-01-0031 terminals or equivalent.

J3 (Speaker Connector) Pinout

Pin #	Signal	Type	Description
1	SP1	Out	Speaker output
2	VCC	—	+5V

J4 (Multi-I/O Connector)

J4 is a 68-pin SCSI-type female multi-I/O receptacle providing a high density connection to the following interfaces:

- LPT
- PS/2 Mouse
- USB†
- Local keyboard
- COM1
- VGA (if PCI VGA interface is loaded)
- COM2

The pin assignments are given in the "J4 (Multi-I/O Connector) Pinout" table following.

Ziatech offers the ZT 90243 Multi-I/O cable that breaks out these signals into standard connector interfaces. Ziatech also offers the ZT 90244 Multi-I/O Ribbon cable for use when the ZT 8908 is operating in ZT 260/310 enclosures.

† The Ziatech BIOS does not directly support USB. This feature requires third party software.

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J4 (Multi-I/O Connector) Pinout

Pin #	Signal	Pin #	Signal
1	COM1-DCD	**35**	COM2-DCD
2	COM1-DSR	**36**	COM2-DSR
3	COM1-RXD	**37**	COM2-RXD
4	COM1-RTS	**38**	COM2-RTS
5	COM1-TXD	**39**	COM2-TXD
6	COM1-CTS	**40**	COM2-CTS
7	COM1-DTR	**41**	COM2-DTR
8	COM1-RI	**42**	COM2-RI
9	COM1-GND	**43**	COM2-GND
10	COM1-VCC	**44**	COM2-VCC
11	LPT-STB	**45**	VIDEO -RED
12	LPT-AFD	**46**	VIDEO-RGND
13	LPT-PD0	**47**	VIDEO- NC
14	LPT-ERR	**48**	VIDEO-GREEN
15	LPT-PD1	**49**	VIDEO-GGND
16	LPT-INIT	**50**	VIDEO-SDA
17	LPT-PD2	**51**	VIDEO-BLUE
18	LPT-SLIN	**52**	VIDEO-BGND
19	LPT-PD3	**53**	VIDEO-HSYNC
20	LPT-GND	**54**	VIDEO-NC
21	LPT-PD4	**55**	VIDEO-VCC
22	LPT-GND	**56**	VIDEO-VSYNC
23	LPT-PD5	**57**	VIDEO-DGND
24	LPT-GND	**58**	VIDEO-SGND
25	LPT-PD6	**59**	VIDEO-SCL
26	LPT-BUSY	**60**	NC
27	LPT-PD7	**61**	KBD-VCC
28	LPT-PE	**62**	KBD-KBCLK
29	LPT-ACK	**63**	KBD-GND
30	LPT-SLCT	**64**	KBD-KBDAT
31	USB-VCC	**65**	MSE-VCC
32	USB-DATA-	**66**	MSE-MSECLK
33	USB-DATA+	**67**	MSE-GND
34	USB-GND	**68**	MSE-MSDAT

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J5 (PCI Mezzanine Local Bus Interface Connector)

J5 is a 175-pin 2 mm x 2 mm female † receptacle providing the PCI local bus interface to optional mezzanine adapters designed for this application. J5 provides a complete 32-bit PCI interface and is CompactPCI compatible. Refer to the *CompactPCI Specification* for details. The pin assignments are given in the "J5 (PCI Mezzanine Local Bus Interface Connector) Pinout" table below.

J5 (PCI Mezzanine Local Bus Interface Connector) Pinout

Pin #	Z	A	B	C	D	E	F
25	GND	5V	NC	NC	3.3V	NC	GND
24	GND	AD[1]	5V	5V	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	GND	C/BE[0]#	GND
20	GND	AD[12]	GND	5V	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	NC	NC	GND	PERR#	GND
16	GND	DEVSEL#	GND	5V	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
14	GND	CLK13	GND	NC	CLK13	NC	GND
13	GND	GNT2#	CLK02	NC	GND	NC	GND
12	GND	REQ1#	GND	GNT1#	CLK13	REQ2#	GND
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	5V	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK02	AD[31]	GND
5	GND	BRSV	NC	RST#	GND	GNT#	GND
4	GND	BRSV	GND	5V	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	NC	NC	NC	GND
1	GND	5V	-12V	NC	+12V	5V	GND
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

Note: Rows 12-14 are not for adapter use. Adapters use pin D6 for CLK, pin A6 for REQ#, and pin E5 for GNT#.

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J6 (Frontplane Interrupt Connector)

J6 is a latching 10-pin (dual 5-pin) male transition connector with 0.1 inch contact spacing. The mating connector is a T&B Ansley #622-1030 or equivalent. Frontplane interrupts are available through this connector. The pin assignments are given in the "J6 (Frontplane Interrupt Connector) Pinout" table. Program the interrupts through Screen 2 of the BIOS Setup utility to be any of the following: 3, 4, 5, 6, 7, 9, 10, 11, 12, or 14.

J6 (Frontplane Interrupt Connector) Pinout

Pin #	Signal	Type	Default
1	GND	Ground	—
2	FP1*	In	Not routed
3	GND	Ground	—
4	FP3*	In	IR 10
5	GND	Ground	—
6	FP5*	In	IR 11
7	GND	Ground	—
8	FP6*	In	Not routed
9	GND	Ground	—
10	FP7*	In	IR 12

Notes:

1. The interrupt levels shown are the default configuration.
2. The frontplane interrupts are active low inputs that are routed through an inverter before being applied to the interrupt controller.

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J7 (Frontplane DMA Connector)

J7 is a 10-pin (dual 5-pin) vertical male header with 0.1 inch contact spacing. Four frontplane DMA channels are available through this connector (configurable through cuttable traces CT37, CT39, CT41-CT44. The pin assignments are given in the "J7 (Frontplane DMA Connector) Pinout" table below. The mating connector is a T&B Ansley #622-1000 or equivalent.

J7 (Frontplane DMA Connector) Pinout

Pin #	Signal	Type	Description
1	DRQ0/5*	In	DMA request 0 or 5
2	DRQ1/6*	In	DMA request 1 or 6
3	DAK0/5*	Out	DMA acknowledge 0 or 5
4	DAK1/6*	Out	DMA acknowledge 1 or 6
5	DRQ3/7	In	DMA request 3 or 7
6	DMAIOW*	Out	I/O write
7	DAK3/7	Out	DMA acknowledge 3 or 7
8	DMAIOR*	Out	I/O read
9	GND	—	Ground
10	TC*	Out	Terminal count

Notes:

1. Channel selection is made with cuttable traces CT37, CT39, CT41-CT44.
2. DMAIOW* and DMAIOR* must be qualified with the respective DMA acknowledge by the DMA I/O slave.

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J8 (Optional Local IDE Connector)

J8 is an optional 44-pin 2mm x 2mm latching male connector for interfacing to the local hard drive. The pin assignments are given in the "J8 (Optional Local IDE Connector) Pinout" table. Ordering option D1 includes an IDE drive integrated with the ZT 8908. This option is useful for single board computer operation (no STD 32 backplane) or for STAR SYSTEM operation where the hard disk interface is local to the ZT 8908.

J8 (Optional Local IDE Connector) Pinout

Pin#	Signal	Type	Description	Pin#	Signal	Type	Description
1	RESET*	Out	Reset	2	GND	—	Ground
3	D7	In/Out	Data Bit 7	4	D8	In/Out	Data Bit 8
5	D6	In/Out	Data Bit 6	6	D9	In/Out	Data Bit 9
7	D5	In/Out	Data Bit 5	8	D10	In/Out	Data Bit 10
9	D4	In/Out	Data Bit 4	10	D11	In/Out	Data Bit 11
11	D3	In/Out	Data Bit 3	12	D12	In/Out	Data Bit 12
13	D2	In/Out	Data Bit 2	14	D13	In/Out	Data Bit 13
15	D1	In/Out	Data Bit 1	16	D14	In/Out	Data Bit 14
17	D0	In/Out	Data Bit 0	18	D15	In/Out	Data Bit 15
19	GND	—		20	KEY	—	Cable Key
21	DREQ*	—	DMA Request	22	GND	—	Ground
23	IOWR*	Out	I/O Write Strobe	24	GND	—	Ground
25	IORD*	Out	I/O Read Strobe	26	GND	—	Ground
27	IORDY	—	I/O Ready	28	ALE	Out	Address Latch En.
29	DACK*	—	DMA Acknowledge	30	GND	—	Ground
31	IRQ	In	Interrupt Request	32	IOCS16 *	In	16-bit I/O handshake
33	A1	Out	Address Bit 1	34	PDIAG	—	Inter-drive diagnostics
35	A0	Out	Address Bit 0	36	A2	Out	Address Bit 2
37	CS0*	Out	Chip Select (1F0h-1FFh)	38	CS1*	Out	Chip Select (3F6h)
39	ACT*	In	Active/Slave present	40	GND	—	Ground
41	VCC	—	+5V - Drive Logic	42	VCC	—	+5V - Drive Motor
43	GND	—	Ground	44	XT/AT	Out	Drive Mode = AT

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J10 (VGA Transition Connector)

J10 is a 16-pin, 2 x 8, 2 mm connector providing an interface for optional PCI VGA interface boards to route video signals to the ZT 8908. This mechanism allows all cabling to be done through the J4 Multi-I/O Connector, including the VGA interface. The zPM11 Super VGA Interface uses this mechanism. The pin assignments are given in the "J10 (VGA Transition Connector) Pinout" table.

J10 (VGA Transition Connector) Pinout

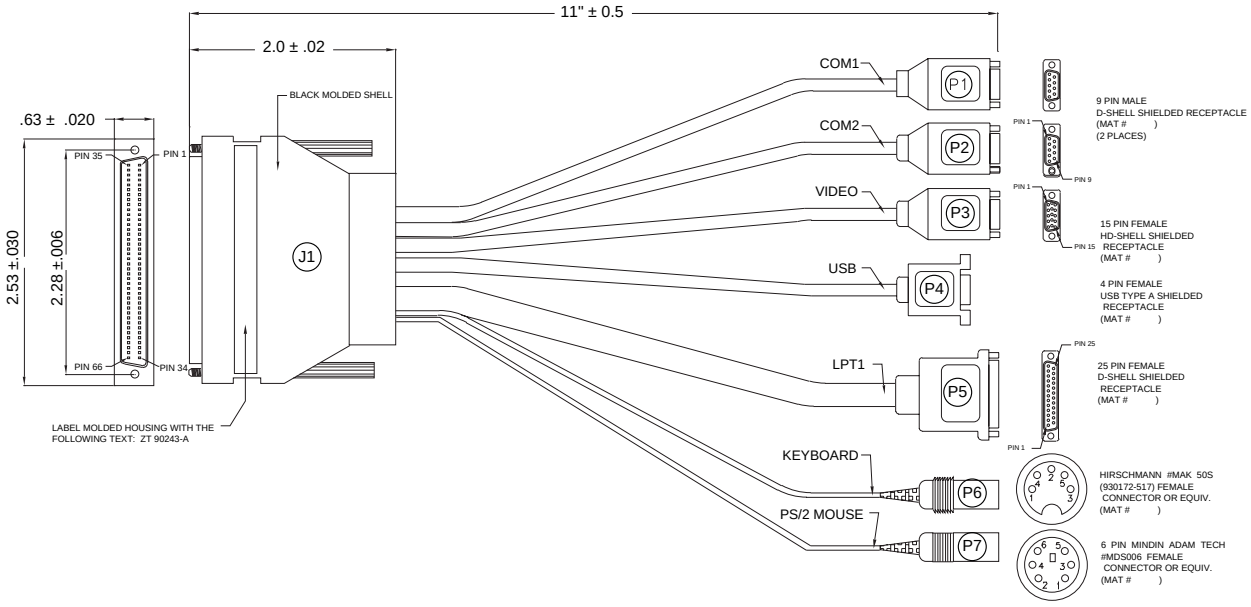
Pin #	Signal	Type	Description
1	RED	Out	VGA Red
2	GRN	Out	VGA Green
3	BLUE	Out	VGA Blue
4	NC	—	No Connect
5	GND	—	Ground (Dig)
6	GND	—	Ground (Red)
7	GND	—	Ground (Green)
8	GND	—	Ground (Blue)
9	NC	—	No Connect
10	GND	—	Ground (Sync)
11	NC	—	No Connect
12	SDA	In/Out	VGA Data
13	HSYNC	Out	VGA Hor. Sync.
14	VSYNC	Out	VGA Ver. Sync.
15	SCL	Out	VGA Data Clock
16	NC	—	No Connect

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Cables

The following cables are available from Ziatech Corporation.

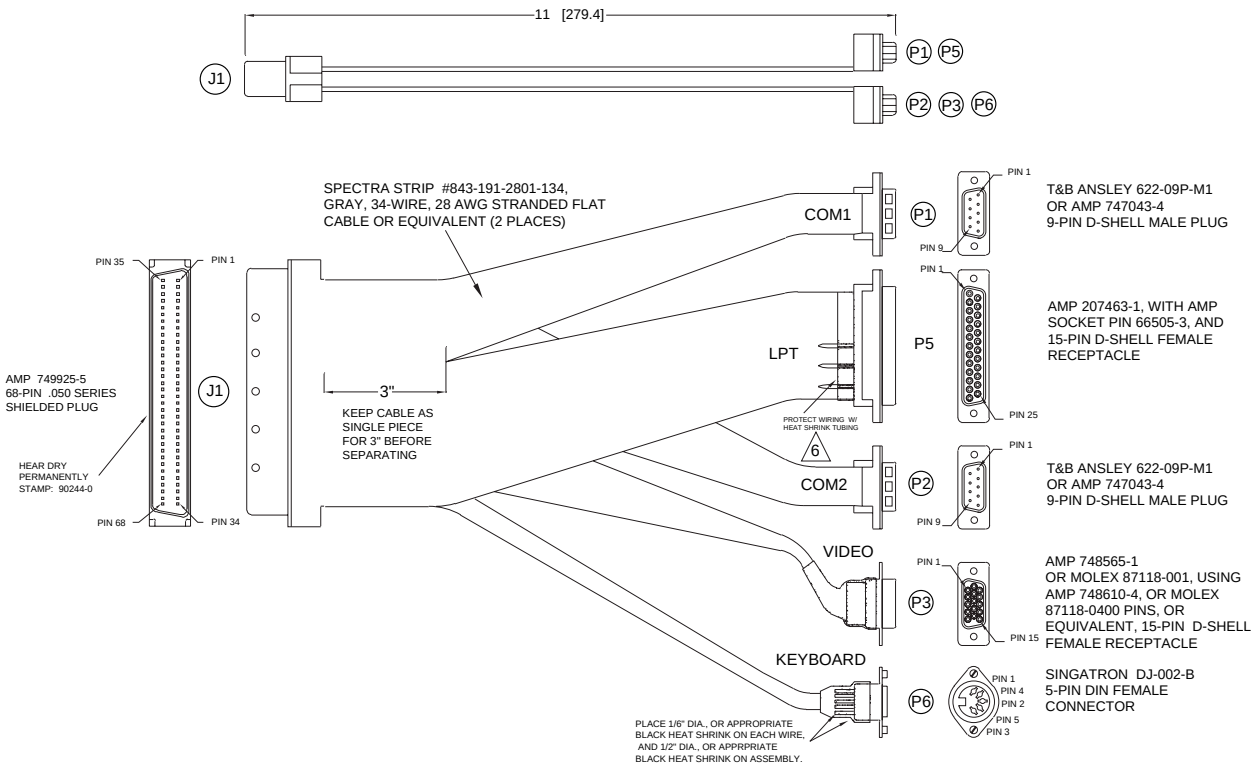
- ZT 90243: 68-pin Multi-I/O cable supporting COM1, COM2, LPT, Video, Keyboard, USB, and PS/2 Mouse
- ZT 90244: 68-pin Multi-I/O ribbon cable supporting COM1, COM2, LPT, Video, and Keyboard



J1– P1 (COM1)	J1– P5 (LPT)		J1– P6 (KYBRD)	J1– P2 (COM2)	J1– P3 (VIDEO)	J1– P4 (USB)
1 - 1	11 - 1	24 - (23, 24, 25, SHIELD)	61 - 5	35 - 1	45 - 1	31 - 1
2 - 6	12 - 14	25 - 8	62 - 1	36 - 6	46 - 6	32 - 2
3 - 2	13 - 2	26 - 11	63 - 4, SHIELD	37 - 2	47 - 11	33 - 3
4 - 7	14 - 15	27 - 9	64 - 2	38 - 7	48 - 2	34 - 4
5 - 3	15 - 3	28 - 12	NC - 3	39 - 3	49 - 7	
6 - 8	16 - 16	29 - 10		40 - 8	50 - 12	
7 - 4	17 - 4	30 - 13	J1– P7 (MOUSE)	41 - 4	51 - 3	
8 - 9	18 - 17		65 - 4	42 - 9	52 - 8	
9 - 5	19 - 5		66 - 5	43 - 5	53 - 13	
10 - NC(+5)	20 - (18, 19, 20, SHIELD)		67 - 3	44 - NC(+5)	54 - 4	
	21 - 6		68 - 1		55 - 9	
	22 - (21, 22, SHIELD)		NC - 2		56 - 14	
	23 - 7		NC - 6		57 - 5	
					58 - 10	
					59 - 15	

ZT 90243 Rev. A Multi-I/O Cable

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J1– P1 (COM1)	J1– P5 (LPT)	J1– P2 (COM2)	J1– P3 (VIDEO)	J1– P6 (KYBRD)
1 - 1	11 - 1	35 - 1	45 - 1	61 - 5
2 - 6	12 - 14	36 - 6	46 - 6	62 - 1
3 - 2	13 - 2	37 - 2	47 - 11	63 - 4, SHELL
4 - 7	14 - 15	38 - 7	48 - 2	64 - 2
5 - 3	15 - 3	39 - 3	49 - 7	NC - 3
6 - 8	16 - 16	40 - 8	50 - 12	65 - NC
7 - 4	17 - 4	41 - 4	51 - 3	66 - NC
8 - 9	18 - 17	42 - 9	52 - 8	67 - NC
9 - 5	19 - 5	43 - 5	53 - 13	68 - NC
10 - NC	20 - 18, 19, 20	44 - NC	54 - 4	
	21 - 6		55 - 9	
	22 - 21, 22,		56 - 14	
	23 - 7		57 - 5	
	24 - 23, 24, 25		58 - 10	
	25 - 8		59 - 15	
	26 - 11		60 - NC	
	27 - 9			
	28 - 12			
	29 - 10			
	30 - 13			
	31 - NC			
	32 - NC			
	33 - NC			
	34 - NC			

ZT 90244 Multi-I/O Ribbon Cable

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C. PCI CONFIGURATION SPACE MAP

All PCI compliant devices contain a PCI configuration header. The generic layout of the header is shown in the "PCI Configuration Header" diagram.

Additionally, a device may contain unique configuration registers (at location > 40h). For the ZT 8908, these are shown in the "ZT 8908 Onboard Device PCI Bus Mapping" table. Details for each device's configuration space can be found in Intel Corporation's data manuals at the following web address: http://developer.intel.com

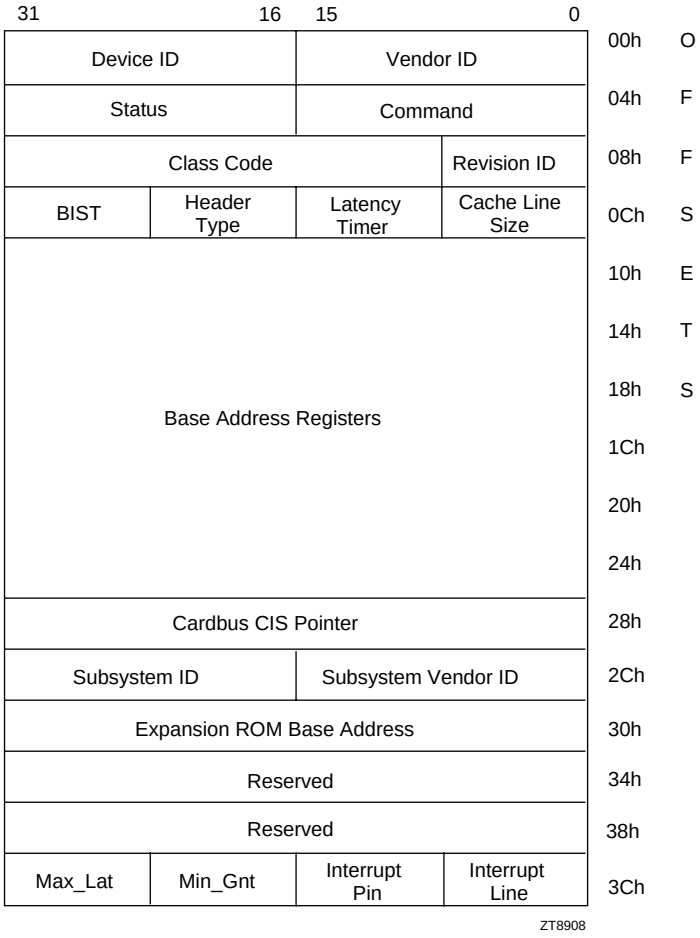
Onboard Device PCI Bus Mapping

Bus # (hex)	Dev # (hex)	Fcn # (hex)	Vendor ID	Device ID	Description
00	00	00	8086	7100	Intel 430 MTXC Controller
00	07	00	8086	7110	Intel 430 PIIX4 PCI-to-ISA Bridge
00	07	01	8086	7111	Intel 430 PIIX4, IDE Interface
00	07	02	8086	7112	Intel 430 PIIX4, USB Interface†
00	07	03	8086	7113	Intel 430 PIIX4, Dynamic Power Management Interface
00	08	00	1138	8905	Ziatech PCI-to-STD Bridge
00	09	00	‡	‡	Mezzanine Connector

† The Ziatech BIOS does not directly support USB. This feature requires third party software.

‡ The vendor and device ID will vary depending upon the device plugged into the mezzanine connector.

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PCI Configuration Header

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D. ZT 8908 VS. ZT 8905: TECHNICAL DIFFERENCES

This appendix describes the technical differences between the ZT 8905 and the ZT 8908 single board computers. It includes information to help existing ZT 8905 customers adapt their applications to the ZT 8908.

ZT 8908 New Features

As shown in the list below, the ZT 8908 incorporates new features that are improvements over the ZT 8905 design.

- An enhanced chipset architecture provided by the Intel 430TX PCIset Interface chip.
- New Intel Pentium Processors with MMX Technology and AMD-K6 MMX Enhanced Processors.
- The ZT 8908 uses industry standard 72-pin SO-DIMM DRAM modules (commonly implemented on laptop computers). Modules may be purchased in 16, 32, or 64 Mbyte sizes allowing for 32 Mbytes minimum and 128 Mbytes maximum onboard memory capacity.
- 512 Kbyte (L2) cache is standard on all board configurations.
- A flash memory "write-protect" switch (SW2-1) physically gates the write line to the flash memory device(s).
- The ZT 8908 implements a more rugged 68-pin high-density SCSI-style multi-I/O connector (J4) on the front of the board. The mating connector screws into place and is available as a standard cable option (ZT 90243). The cable includes connectors for onboard peripherals as shown in the "ZT 8908 / ZT 8905 Cabling Comparison" table. Note that the PS/2-style mouse port and the Universal Serial Bus (USB) † port are new features not available with the ZT 8905.
- The ZT 8908 provides onboard frontplane interrupt (J6) and DMA (J7) connectors, whereas the ZT 8905 provided these interfaces via a cable connected to its multi-I/O connector. The ZT 8908 also provides a speaker interface; the ZT 8905 did not.

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ZT 8908 / ZT 8905 Cabling Comparison

Peripheral Device	ZT 8908 Multi-I/O Cable (ZT 90243)	ZT 8905 Multi-I/O Cable (ZT 90205)
COM1 Serial	9-pin male D-shell	Same
COM2 Serial	9-pin male D-shell	Same
LPT1 Printer	25-pin female D-shell	Same
VGA Video	15-pin female D-shell	Same
Keyboard	5-pin female DIN (AT) keyboard	Same
PS/2 Mouse	6-pin female mini-DIN mouse	Not available
Universal Serial Bus (USB)	4-pin female Type A USB	Not available

ZT 8908 Programming Issues

In most cases, ZT 8905 applications that do not program any ALI chipset registers or flash memory ports directly will not require modification in order to run on the ZT 8908.

Unchanged configurable items include:

- The COM1, COM2, LPT1, and Timer/Counters peripherals are in the same I/O locations on both boards.
- The available interrupt routing selections are the same on both boards.
- Software configuration of interrupt routing (via the BIOS SETUP utility) is similar on both boards.

Device and/or mapping differences on the ZT 8908 include:

- Chipset: Intel 430TX PCIset
- Flash memory: Up to two 2 Mbyte Intel flash devices may be factory installed. Flash memory will be mapped as 16 256 Kbyte pages accessible from FFF8000h - FFFBFFFh and FFFC000h - FFFFFFFFh (BIOS).
- I/O Map Changes: There are some differences between the ZT 8905 and ZT 8908 I/O maps. Compare the I/O maps in the respective manuals to learn these differences.

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Backplane Keyboard

Unlike the ZT 8905, the ZT 8908 does not support a backplane keyboard controller (such as that provided on the ZT 8982 Video/Keyboard Interface). The keyboard interface for the ZT 8908 is accessible through the multi-I/O connector (J4) at the front of the board.

ZT 260 and ZT 310 Enclosures

Listed below are the new options added to the ZT 2502 and ZT 2503 front plates to support the ZT 8908 video/keyboard connector.

- ZT 2502-V10: System Plate for ZT 8908 (single CPU system)
- ZT 2503-V10: Video/Keyboard Access Plate for a single ZT 8908 (STAR SYSTEM temporary master)

RELIABILITY

Ziatech has taken extra care in the design of the ZT 8908 in order to ensure reliability. The product was designed in top-down fashion, using the latest in hardware and software design techniques, so that unwanted side effects and unclean interactions between parts of the system are eliminated. Each ZT 8908 has an identification number. Ziatech maintains a lifetime data base on each board and the components used. Any negative trends in reliability are spotted and Ziatech's suppliers are informed and/or changed.

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E. CUSTOMER SUPPORT

This appendix offers technical assistance and warranty information for this product, and also the necessary information should you need to return a Ziatech product.

TECHNICAL/SALES ASSISTANCE

If you have a technical question, please call Ziatech's Customer Support Service at the number below, or e-mail our technical support team at tech_support@ziatech.com. Ziatech also maintains an FTP site located at ftp://ziatech.com/Tech_support.

If you have a sales question, please contact your local Ziatech Sales Representative or the Regional Sales Office for your area. Address, telephone and FAX numbers, and additional information are available at Ziatech's website, located at http://www.ziatech.com.

Corporate Headquarters

1050 Southwood Drive

San Luis Obispo, CA 93401 USA

Tel (805) 541-0488

FAX (805) 541-5088

RELIABILITY

Ziatech takes extra care in the design of the product in order to ensure reliability. The product was designed in top-down fashion, using the latest in hardware and software design techniques, so that unwanted side effects and unclean interactions between parts of the system are eliminated. Each product has an identification number. Ziatech maintains a lifetime data base on each board and the components used. Any negative trends in reliability are spotted and Ziatech's suppliers are informed and/or changed.

RETURNING FOR SERVICE

Before returning any of Ziatech's products, you must phone Ziatech at (805) 541-0488 and obtain a Return Material Authorization (RMA) number. Please supply the following information to Ziatech in order to receive an RMA number:

- Your company name and address for invoice
- Your shipping address and phone number
- The product I.D. number
- The name of a technically qualified individual at your company familiar with the mode of failure

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Once you have an RMA number, follow these steps to return your product to Ziatech:

1. Contact Ziatech for pricing if the warranty expired.
2. Supply a purchase order number for invoicing the repair if the warranty expired.
3. Pack the board in **anti-static** material and ship in a sturdy cardboard box with enough packing material to adequately cushion it.

Note: Any product returned to Ziatech improperly packed will immediately void the warranty for that particular product!

4. Mark the RMA number clearly on the outside of the box.

ZIATECH WARRANTY

Warranty information for Ziatech products is available at Ziatech's website, located at http://www.ziatech.com.

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