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ZT 8954



Low Profile
Floppy Disk Controller

Hardware User Manual

ZIATECH CORPORATION

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MANUAL ORGANIZATION

This manual describes the operation and use of the ZT 8954 Low Profile Floppy Disk Controller. The following outline summarizes the focus of each section in this manual.

Chapter 1, "Introduction," offers an overview of the ZT 8954. It includes a product definition, a list of product features, a functional block diagram, and a brief description of each block. This chapter is most useful to those who wish to compare the features of the ZT 8954 against the needs of a specific application.

Chapter 2, "Getting Started," summarizes the information you need to get your ZT 8954 operational. This includes system requirements and installation instructions.

Chapter 3, "Theory of Operation," presents an operational view of the ZT 8954's hardware. Each of the board's functions is described in detail, and some common concerns are addressed.

Chapter 4, "FDC Description (82078)," defines the 82078 Floppy Disk Controller (FDC) and describes its functions and capabilities in detail.

Appendix A, "Jumper Configurations," describes all of the ZT 8954 jumpers in detail, specifies factory default settings, and provides the information you need to tailor your board to a specific application.

Appendix B, "Specifications," contains the electrical, mechanical, and environmental specifications.

Appendix C, "Customer Support," offers technical support information, the Ziatech warranty, and instructions for returning the ZT 8954 if service is necessary.

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1. INTRODUCTION

This chapter provides a brief introduction to the ZT 8954 Low Profile Floppy Disk Controller. It includes a product definition, a list of product features, a functional block diagram, and a description of each function. You will find unpacking information and installation instructions in Chapter 2, "Getting Started."

PRODUCT DEFINITION

The ZT 8954 is a Low Profile Floppy Disk Controller for the STD 32 bus structure. Support is provided for 5¼" and 3½" floppy drives, as well as floppy controller-compatible tape drive units.

The ZT 8954 is available with an integrated 3½" slimline drive (occupying just one STD 32 card slot), as a remote mount option with no drive loaded, and with a mounting bracket to extend the drive out for use in card cages with front bezels (for example, the ZT 250).

Mechanically, the ZT 8954 is compatible with both the STD and the STD 32 bus specifications. The ZT 8954 supports 5 and 8 MHz bus operation.

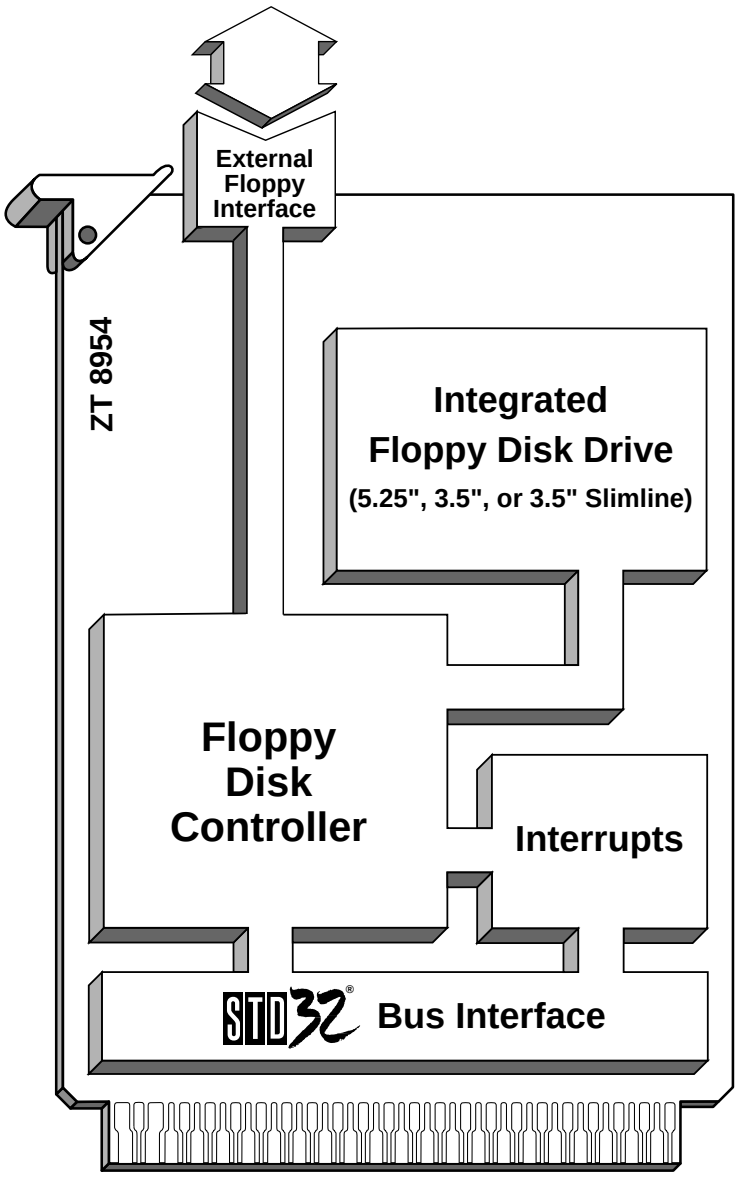
FEATURES

- STD 32 bus compatible
- 360K, 720K, 1.2 Mbyte, and 1.44 Mbyte floppy disk drive support
- IBM-PC®/AT®/MCA®/EISA® compatible register set
- 3½", 5¼" floppy disk drive support
- Integrated 3½" slimline floppy disk drive (1 slot usage) (ZT 8954-D1)
- Remote mounting option (20") (ZT 8954-D0)
- Tape drive support
- Bracket mounting option for ZT 250/300 card cages (ZT 8954-D1M)
- STD-80 backplane option (ZT 8954-D3)
- Burned in at 55º C and tested to guarantee reliability
- STD 32 compliance:
- I/O Slave: SA8-I, IXL, IXP, SDMA8, SDMABP, EDMAA, EDMAB
- Five-year warranty

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FUNCTIONAL BLOCKS

The "Functional Block Diagram" below illustrates the board's major functional blocks. A description of the board's features and functional blocks can be found in the following topics.



Functional Block Diagram

STD 32 Bus Interface

STD bus interface logic decodes the I/O address for cycles destined for the floppy disk controller. Control of the backplane data bus buffer is also performed in this logic for both programmed I/O cycles and DMA cycles.

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Interrupts

The Floppy Disk Controller (FDC) communicates status to the host processor via an interrupt. This interrupt is routed through a group of jumpers to select the appropriate backplane interrupt to drive. Standard bussed interrupts are supported, as well as the slot-specific interrupt for STD 32 backplanes. By default, the floppy disk controller drives INTRQ2* on the backplane, which is normally connected on the host CPU to IR6.

Floppy Disk Controller

The Floppy Disk Controller used on the ZT 8954 supports all DOS-compatible floppy disk drives through either a 0.1" 34-pin header or a 1-millimeter 26-pin connector. Data rates of 250 Kbytes, 300 Kbytes, 500 Kbytes, and 1 Mbytes per second are supported through program control. Perpendicular recording mode is supported for 2.88 Mbyte floppy disk drives. An on-board 16-byte FIFO provides increased bus-latency tolerance. The FDC is fully compatible with the IBM-AT, IBM-PS/2®, and EISA architectures. The FDC supports up to two disk drives directly.

Floppy Disk Drive

The ZT 8954 supports a variety of floppy disk drives. Two types of connectors are provided for interfacing to the different styles of floppy drives. A 34-pin 0.1" header interfaces to older style 5¼" and 3½" drives. For newer 3½" slimline drives, a 26-pin 1 mm FPC connector is provided.

External Floppy Interface

The ZT 8954 supports remote mounted floppy drives through an onboard 34-pin 0.1" header.

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2. GETTING STARTED

This chapter discusses features of the ZT 8954 and summarizes the information you need to get your ZT 8954 operational. Read this chapter and Chapter 3, "Theory of Operation," before you use the board. Most users will not need to adjust any jumpers for correct operation.

Many of the topics in "Getting Started" are discussed in greater detail in subsequent chapters. You will find a number of cross references for topics containing further information. Many of the details of the floppy disk controller can be found in the Intel *Peripherals Data Book* in the *82078-1* data sheet, also available as a separate Intel publication 290468-002.

The ZT 8954 is supported by CPU boards that have on-board DMA controllers to perform the floppy disk data transfer (for example, ZT 8902 Revision A, ZT 8903, ZT 8904, and ZT 8905). The ZT 8954 is supported in Ziatech DOS and STD 32 STAR SYSTEMs, starting with BIOS 4.01.

UNPACKING

Be sure to check the shipping carton for damage. If the shipping carton and contents were damaged, notify the carrier and Ziatech for an insurance settlement. Retain the original shipping carton and packing material for inspection by the carrier. Save the anti-static bag for storing or returning the ZT 8954.

Do not return any product to Ziatech without a Return Material Authorization (RMA) number. The procedure for obtaining an RMA number from Ziatech is explained in the "Returning for Service" section of Appendix C, "Customer Support."



Caution: Like all equipment utilizing MOS devices, the ZT 8954 must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the ZT 8954 to handle the board.

SYSTEM REQUIREMENTS

The ZT 8954 is designed for use in STD and STD 32 bus environments. The ZT 8954 is dependent upon the host CPU's performing DMA cycles to transfer data between the floppy disk and the host's memory. It is important to note that not all CPU boards have this capability. In particular, the ZT 8954 is designed for use with the ZT 8902 Revision A, ZT 8903, ZT 8904, and ZT 8905. Use the following lists to determine whether your Ziatech CPU board supports the ZT 8954.

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CPU Boards supporting the ZT 8954:

Note: As CPU boards are designed, this list will change. Contact Ziatech for details on boards not listed here.

- ZT 8902 Revision A
- ZT 8903
- ZT 8904
- ZT 8905

CPU Boards NOT supporting the ZT 8954:

Note: As CPU boards are designed, this list will change. Contact Ziatech for details on boards not listed here.

- ZT 8801/88CT01
- ZT 8802/88CT02
- ZT 8808/8809/88CT09
- ZT 8816/8817
- ZT 8901/89CT01
- ZT 8902 Revision 0.X
- ZT 8910
- ZT 8911 Revision 0.X (although slot-specific DMA can be used)

Physical Requirements

The ZT 8954-D1 and ZT 8954-D0 require just one STD 32 card cage slot. The maximum board height, including the floppy disk drive, is 0.5". Note that boards placed to the left of the ZT 8954 should be chosen with care so that they do not exceed the maximum height limit. Should this happen, select another board to install next to the ZT 8954. Note that the top of the floppy disk drive is shielded to protect against shorting adjacent boards.

The ZT 8954-D3 requires three STD card slots. Refer to the "Card Dimensions and Weight" section of Appendix B, "Specifications," for exact dimensions of the ZT 8954.

Power Requirements

Power required by the ZT 8954 depends upon the type of drive loaded on the controller. Consult Appendix B, "Specifications," for details. In general, the ZT 8954 and drives shipped with it do not require +12 V. Only +5 V is required for the complete assembly. Some older drives do use +12 V, and they can be powered through the ZT 8954 via the J5 power connector.

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Environmental Requirements

Ziatech recommends vertical mounting for applications in which a fan is not used. Horizontal mounting requires a minimum air flow of 30 cubic feet/minute passing over the surface of the board.

INSTALLING THE ZT 8954

If the ZT 8954 is purchased as part of a system, then the system-specific jumpers will already have been installed at the factory. In general, you should not need to change the jumpers on the ZT 8954. The ZT 8954 is, by default, set up to drive INTRQ2* (P50) on the STD 32 backplane, and will use Mode 2 DMA (BUSRQ*/BUSAK*, backplane control signals) for DOS applications. The default jumper configuration for Ziatech CPU boards also reflects this configuration.

If the ZT 8954 is purchased as a stand-alone control (for remote mounting of the floppy drive), then you may need to change the floppy interface jumpers to meet the particular requirements of the floppy disk drive you are using. In particular, older 5¼" drives have an inverted DENSEL* signal when compared to the 3½" drives. Jumpers W6 and W7 let you select the sense of this signal. By default, W7 is in; this selects the proper logic level for DENSEL* for 3½" drives. Refer to the description of W7 in Appendix A, "Jumper Configurations," for details.

Interrupt Selection

Jumpers W12-18 select the backplane pin to which the floppy disk controller interrupt will be driven. By default, INTRQ2* (backplane pin P50) is used for floppy disk subsystem interrupts. Other backplane interrupts, as well as STD 32 slot-specific interrupts, can be selected if the default is not acceptable. The slot-specific interrupt is configurable for either active low (IXL) or positive edge (IXP).

DMA Mode Selection

The ZT 8954 uses four different modes for floppy DMA transfers (Modes 0-3). The primary mode of operation is Mode 2, which uses the BUSRQ*/BUSAK* signals for bus arbitration and uses the backplane control signals (DMAIOW*, DMAIOR*, and T-C) for the data transfer. Slot-specific DMA and frontplane DMA can also be selected depending upon the capabilities of the host CPU board. Jumpers W1 and W2 select the DMA Mode for the ZT 8954.

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Jumper Requirements - DOS and STD 32 STAR SYSTEMs

Installed:

W2, W4, W5, W7, W9, W10, W16

Not installed:

W1, W3, W6, W8, W11-15, W17, W18

This configuration selects DMA Mode 2, drives INTRQ2* with the floppy disk interrupt, and sets up the floppy disk drive interface for 3½" drives.

Refer to Appendix A, "Jumper Configurations," for details.

FRONTPLANE CONNECTORS

As shown in the "Connector Locations" drawing, the ZT 8954 includes six frontplane connectors to interface to application-specific devices. A brief description of each connector is given below in the "Frontplane Connector Assignments" table. For more information, see the "Connectors" topic in Appendix B.

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Frontplane Connector Assignments

Connector	Function
J1	J1 provides Direct Memory Access (DMA) support for external peripherals via channel 0 or 3 on the local 8237A DMA controller. The floppy disk controller can use this connector to request service from the DMA controller on the ZT 8954. This connector is not normally loaded on the ZT 8954, as it resides under the integrated floppy drive.
J2, J3	J2 and J3 accommodate 0.1" 34-pin floppy interface drives. J3 is a reverse image of J2 to allow interfacing to drives with minimal cable twisting.
J4, J6	J4 and J6 are 1 mm FPC cable connectors for newer slimline floppy disk drives. J4 is not loaded by default as it is underneath the integrated floppy drive.
J5	J5 is for a power cable connection location for remote floppy disk drives.

STD 32 COMPLIANCE

STD 32 peripherals are required to meet certain compliance standards. This allows the system integrator to match capabilities among different manufacturers' boards.

STD 32 peripherals are available from a variety of manufacturers.

The ZT 8954 has the following STD 32 compliance:

I/O Slave: SA8 - I, IXP, IXL, SDMA8, SDMABP, EDMAA, EDMAB

Definitions

SA8	Standard Architecture 8-bit transfers
I	Can drive INTRQ*, INTRQ1*, INTRQ2*, and/or INTRQ3*
IXP	Can drive IRQx with a positive active edge
IXL	Can drive IRQx with an active low request
SDMA8	Supports frontplane 8-bit DMA transfers
SDMABP	Supports Standard Architecture backplane DMA by BUSRQ*/BUSAK*
EDMAA	Extended Architecture type A DMA transfers supported
EDMAB	Extended Architecture type B DMA transfers supported

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3. THEORY OF OPERATION

This chapter presents an operational overview of the hardware operation of the ZT 8954. Each of the board's functions is described in detail. Frequently asked questions are addressed below.

FREQUENTLY ASKED QUESTIONS

Why is the ZT 8954 Incompatible With Older CPU Boards?

The ZT 8954 relies upon the host CPU to perform DMA transfers between the floppy disk controller and the host CPU's memory. Only boards that can field requests from a DMA slave (for example, ZT 8902) can be used with the ZT 8954. Many older CPU boards do not have on-board DMA controllers or do not allow for off-board DMA slaves. With STD 32, DMA capability was added by defining the backplane signals necessary for data transfer completion under DMA. The ZT 8954 is not supported by the ZT 8801, ZT 8802, ZT 8808, ZT 8809, ZT 8816, ZT 8817, ZT 8901, ZT 8902 Revision 0.X, or ZT 8911 Revision 0.X.

What Floppy Disk Drives are Supported by the ZT 8954?

The ZT 8954 supports all floppy disk drives that are compatible with the IBM-PC family. Data transfer rates of 250 Kbps through 2 Mbps are supported. In addition, the ZT 8954 supports tape drive units that are floppy interface compatible, such as the Colorado Memory Systems "JUMBO" tape drives.

How Do I Use Frontplane DMA?

The ZT 8954 is capable of frontplane DMA, but only as a special option from Ziatech (ZT 8954-D3). The connector location for frontplane DMA is located underneath the integrated 3½" drive. In order to minimize slot usage by the floppy subsystem, this connector is not loaded. Frontplane DMA is primarily used for floppy operation in STD-80 card cages that have no backplane DMA capability. When the frontplane DMA connector is loaded, the floppy disk drive must be raised; this causes the complete ZT 8954/Floppy Disk Drive to occupy two card slots.

How Do I Remote Mount A Floppy Disk Drive?

Floppy Disk Drives can be remote mounted with a ZT 8954-D0 board and the addition of two cables, ZT 90077 and ZT 90172. These cables allow for interfacing drives up to 20" away from the controller. These cables support 3½" and 5¼" drives with separate power connectors and drives that use the older style .050" ribbon cable for floppy drive control (34-pin 0.1" connectors). The micro-floppy 3½" drives that use FPC cable are not supported by this mechanism. These drives can be interfaced with a 26-pin FPC cable on 1 millimeter pitch at up to 0.5 meters or less. Parlex company (telephone

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[603] 893-0040) manufactures custom length cables for these drives for your application. When interfacing to remote drives, minimize the amount of electrical noise in the system to avoid corrupting the data transfer between the floppy disk drive and the floppy disk controller.

STD BUS COMPATIBILITY

The ZT 8954 is fully compatible with both the STD-80 and STD 32 bus specifications. STD 32 is a superset of STD-80. Both specifications are available through Ziatech.

STD BUS INTERFACE

The ZT 8954 interfaces the STD and STD 32 bus structure to IBM-PC platform floppy disk controllers. Programmed I/O transfers are used to program the ZT 8954 for a floppy disk sector read or write. DMA is used for the transfer of floppy disk data. DMA can be done a byte at a time (which is the IBM PC method); or, with the on-board 16-byte FIFO, the ZT 8954 can perform block DMA in order to improve bus-latency tolerance. Under MS-DOS, floppy disk transfers also require the use of an interrupt, which is nominally jumpered for INTRQ2* on the backplane. The ZT 8954 uses BUSRQ*/BUSAK* and backplane DMA control signals, by default, for data transfers.

Data Transfers

The floppy disk controller supports both polled and DMA-driven data transfers. Standard MS-DOS uses DMA, by default, for moving data back and forth between the host CPU's memory and the floppy disk controller. The DMA transfer is driven by the DMA controller on board the host CPU board. The ZT 8954 does not have a controller. The BIOS software is responsible for managing the low-level hardware in DOS systems and in STD 32 STAR SYSTEM™ multiprocessing applications. All transfers are 8 bits wide. The normal DMA transfer mechanism is to use BUSRQ* to request a DMA cycle, qualify DMAIOW* or DMAIOR* with BUSAK* to transfer data, and receive T-C as a terminal count signal from the host CPU. This is referred to as Mode 2 DMA for the ZT 8954. Slot-specific DMA, frontplane DMA, and a combination of frontplane and backplane DMA can also be selected as other modes.

Memory

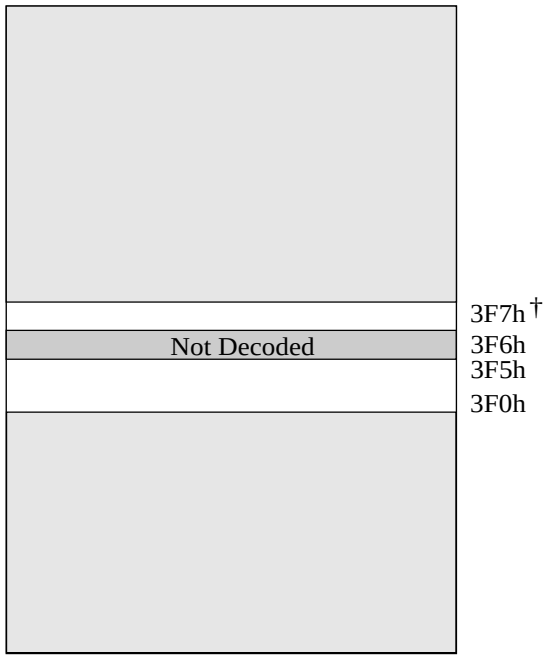
The ZT 8954 does not occupy or decode any of the STD bus memory address space.

I/O

The ZT 8954 decodes the I/O address range 3F0h-3F7h, with the exception of 3F6h. Port 3F7h is shared with the hard disk interface (ZT 8952/8953); only one bit is driven by the ZT 8954 when that port is read by the host CPU. The other seven bits are driven

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by the ZT 8952/8953. The ZT 8954 is not jumper selectable for any alternate I/O address. The I/O map is shown below in the "I/O Map" figure.



† 3F7h is shared with the ZT 8952/53.

I/O Map

Floppy Disk Controller Registers

The Floppy Disk Controller (FDC) interface is composed of eight registers. The "Floppy Disk Controller I/O Registers" table defines the I/O address for all of the FDC registers. These registers are further described in Chapter 4, "FDC Description (82078)."

Floppy Disk Controller I/O Registers

I/O Port Address	I/O Read Function	I/O Write Function
3F0h	Status Register A	--
3F1h	Status Register B	Status Register B
3F2h	Digital Output Register	Digital Output Register
3F3h	Tape Drive Register	Tape Drive Register
3F4h	Main Status Register	Data Rate Select Register
3F5h	Data	Data
3F6h	Reserved	Reserved
3F7h	Digital Input Register†	Configuration Control Register

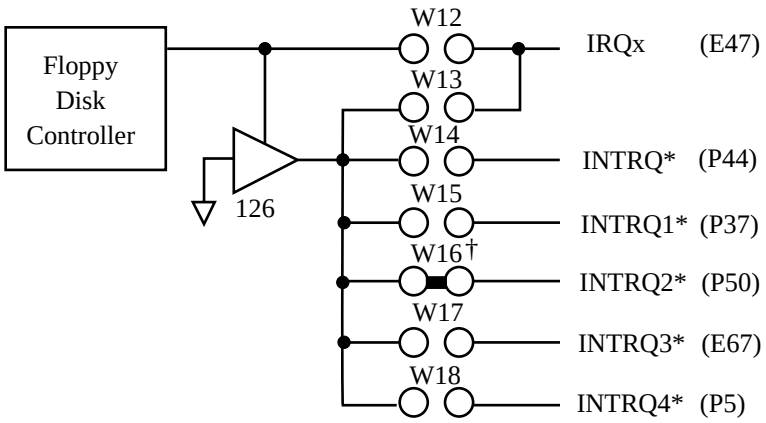
† Bit 7 only driven

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INTERRUPTS

The ZT 8954 can drive any of the bussed backplane interrupts, as well as the slot-specific interrupt IRQx. By default, the ZT 8954 is jumpered for driving INTRQ2* (backplane pin P50) for the floppy disk subsystem interrupt.

The "Interrupt Selections" illustration below indicates the possible interrupt selections.



† W16 is installed by default.

Interrupt Selections

ZIATECH STD 32 STAR SYSTEM USE

In multiprocessing operations, the floppy disk interface is shared between CPUs in the backplane. Because different CPU boards are supported by different floppy disk interfaces, the STD 32 STAR SYSTEM allows for different CPU board types. When a system is composed of different CPU types, a simple rule is applied, as detailed in the following topic, "STAR SYSTEM Floppy Rule".

STAR SYSTEM Floppy Rule

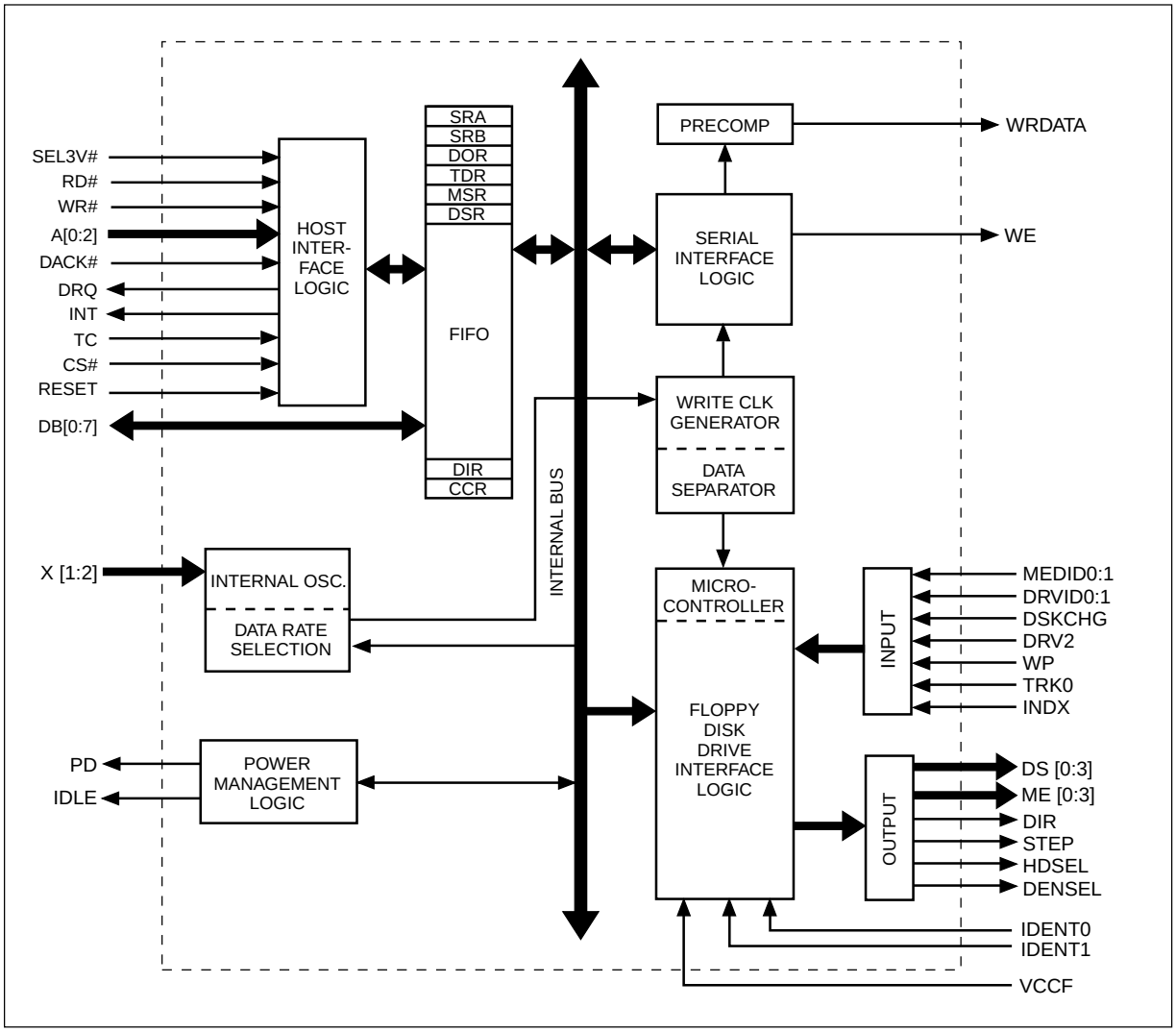
Always match the floppy disk controller to the Permanent Master type. For instance, if the ZT 8902 Rev A is your Permanent Master, the ZT 8954 is required. The STAR BIOS will manage transfers between Temporary Masters and the floppy disk through the Permanent Master.

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4. FDC DESCRIPTION (82078)

The 82078 is a true single-chip floppy disk controller for IBM PC/AT and PS/2 architectures. The integrated analog data separator needs no external compensation, yet allows for a wide motor speed variation with exceptionally low soft error rates. The microprocessor interface has 100% hardware register compatibility for PC/ATs and PS/2s. The 16-byte FIFO with programmable thresholds is extremely useful in multiple master systems or systems with a large amount of bus latency.

The following "82078 Block Diagram" below shows a block diagram of the 82078 floppy disk controller.



82078 Block Diagram

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PERPENDICULAR RECORDING MODE

An added capability of the 82078 is the ability to interface directly to perpendicular recording floppy drives that use the Toshiba format. Perpendicular recording differs from the traditional longitudinal method by orienting the magnetic bits vertically. This scheme then packs in more data bits for the same area.

The 82078 with perpendicular recording drives can, at a minimum, read standard 3½" floppies as well as read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive. A single command puts the 82078 into perpendicular mode. All other commands operate as they normally do. The perpendicular mode requires the 1 Mbps data rate of the 82078. At this data rate, the FIFO eases the host interface bottleneck due to the speed of data transfer to or from the disk, if utilized.

STATUS, DATA, AND CONTROL REGISTERS

The following topics discuss the status, data, and control registers of the 82078 FDC.

The base address range is supplied via the CS* pin. For PC-compatible designs, this is 3F0h to 3F7h. The following "82078 Register Summary" table summarizes addressing for the status, data, and control registers.

82078 Register Summary

A2	A1	A0	Register
0	0	0	SRA - Status Register A
0	0	1	SRB - Status Register B
0	1	0	DOR - Digital Output Register
0	1	1	TDR - Reserved (Tape Drive Register)
1	0	0	MSR - Main Status Register
1	0	0	DSR - Datarate Select Register
1	0	1	FIFO - Data (FIFO)
1	1	0	Reserved (Not decoded)
1	1	1	DIR - Digital Input Register (Read)
1	1	1	CCR - Configuration Control Register (Write)

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Status Register A (SRA)

3F0h Default

This register is read-only and monitors the state of the interrupt pin and several disk interface pins. This register is part of the PS/2 register set.

7	6	5	4	3	2	1	0
INT PENDING	DRV2*	STEP	TRK0*	HDSEL	INDX*	WP*	DIR

Status Register A

The **INT PENDING** bit is used by software to monitor the state of the 82078 INTERRUPT pin. As a read-only register, no default value is associated with a reset other than that some drive bits change with a reset. The **INT PENDING**, **STEP**, **HDSEL**, and **DIR** bits are low after reset.

Status Register B (SRB)

3F1h Default

This register is read-only and monitors the state of several disk interface pins. This register is part of the PS/2 register set.

7	6	5	4	3	2	1	0
1	1	DRIVE SEL0	WRDATA TOGGLE	RDDATA TOGGLE	WE	MOT EN1	MOT EN0

Status Register B

As the only drive input, **RDDATA TOGGLE**'s level always reflects the level as seen on the cable.

The two **TOGGLE** bits do not read back the state of their respective pins directly. Instead, the pins drive a flip-flop which produces a wider and more reliably read pulse. **Bits 6 and 7** are undefined and always return a 1.

After any reset, the activity on the **TOGGLE** pins is cleared. **Drive select** and **motor** bits are cleared by the RESET pin and not by software resets.

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Digital Output Register (DOR)

3F2h Default

The Digital Output Register contains the drive select and motor enable bits, a reset bit, and a DMAGATE* bit. This register is used in both PC/AT and PS/2 designs. The 8954 is shipped with the IDENT pin in PS/2 configuration.

7	6	5	4	3	2	1	0
MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMA GATE*	RESET	DRIVE SEL1	DRIVE SEL0

Digital Output Register

Bits 4-7, the **MOT ENx** bits, directly control their respective motor enable pins (ME0-3). A 1 means the pin is active. **Bits 0 and 1,** the **DRIVE SELx** bits, are decoded to provide four drive select lines; only one may be active at a time. Since the ZT 8954 ties INVERT low, these signals are active low on the interface. Standard programming practice is to set both MOT ENx and DRIVE SELx bits at the same time. The "Drive Activation Values" table lists a set of DOR values to activate the drive select and motor enable for each drive.

Bit 3, the **DMAGATE*** bit, is not enabled on the ZT 8954. DMAGATE* has no effect upon the INT and DRQ pins, and they are always active.

Bit 2, the **RESET*** bit, clears the basic core of the 82078 and the FIFO circuits. Once set, it remains set until you clear it. This bit is set by a chip reset and the 82078 is held in a reset state until you clear this bit. The RESET* bit has no effect upon this register. The RESET* pin clears this register.

Drive Activation Values

Drive	DOR Value
0	1Ch
1	2Dh
2	4Eh
3	8Fh

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Tape Drive Register (TDR)

3F3h Default

This register allows you to assign tape support to a particular drive during initialization. Any future reference to that drive number automatically invokes tape support. This register is cleared by a hardware reset; software resets have no effect. Bits 2-7 are part of the "enhanced" tape drive register and are made available only when the EREG EN bit is set; otherwise, the bits are not driven.

7	6	5	4	3	2	1	0
MEDID1	MEDID0	DRVID1	DRVID0	BOOTSEL1	BOOTSEL0	TAPESEL1	TAPESEL0

Tape Drive Register

Bits 2 through 7 are not writable and remain three-stated if read when EREG EN is not set. **Bits 4 through 7** are not writable, but return the states of the DRVID0, DRVID1, MEDID0, and MEDID1 pins when EREG EN is set. The EREG EN bit is part of the COMMAND SET and can be found in the 82078 data sheet.

Bits 0 and 1, the **TAPESEL0** and **TAPESEL1** bits, allow you to select which drive is to be configured for tape drive support, as shown in the "Tape Drive Register Selection" table. The Tape Select bits are hardware RESET to 0, making Drive 0 not available for tape support. Drive 0 is reserved for the floppy boot drive on reset.

Bits 2 and 3, the **BOOTSEL0** and **BOOTSEL1** bits, are not reset by software resets and are decoded as shown in the "Boot Drive Selection Options" table. These bits allow for reconfiguring the boot-up drive and are reset only by a hardware reset. A drive can be enabled by remapping the internal DS0 and ME0 nodes to one of the other drive select and motor enable lines. Once a non-default value for BOOTSEL1 and BOOTSEL0 is selected, all programmable bits are virtual designations of drives; it is the user's responsibility to know the mapping scheme in the following table.

Tape Drive Register Selection

TAPESEL1	TAPESEL0	Drive Selected
0	0	None
0	1	1
1	0	2
1	1	3

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Boot Drive Selection Options

BOOTSEL1	BOOTSEL0	Mapping:
0	0	DS0 --> FDS0, ME0 --> FDME0 DS1 --> FDS1, ME1 --> FDME1 DS2 --> FDS2, ME2 --> FDME2
0	1	DS0 --> FDS1, ME0 --> FDME1 DS1 --> FDS0, ME1 --> FDME0 DS2 --> FDS2, ME2 --> FDME2
1	0	DS0 --> FDS2, ME0 --> FDME2 DS1 --> FDS1, ME1 --> FDME1 DS2 --> FDS0, ME2 --> FDME0
1	1	Reserved

Datarate Select Register (DSR)

3F4h Default

This register is included for compatibility with the 82072 floppy controller and is write-only. Changing the data rate changes the timings of the drive control signals. Therefore, to avoid violating drive timings when changing data rates, choose a drive timing such that its fastest data rate will not violate the timing.

7	6	5	4	3	2	1	0
S/W RESET	POWER DOWN	PDOSC	PRE-COMP 2	PRE-COMP 1	PRE-COMP 0	DRATE SEL1	DRATE SEL0

Datarate Select Register

Bit 7, S/W RESET, behaves the same as DOR RESET except that this reset is self-clearing.

Bit 6, POWER DOWN, deactivates the internal clocks and shuts off the oscillator. Disk control pins are put in an inactive state. All input signals must be held in a valid state (D.C. level 1 or 0). POWER DOWN is exited by activating one of the reset functions.

Bit 5, the **PDOSC** bit, is used to implement crystal oscillator power management. The internal oscillator in the 82078 can be programmed to be powered either on or off via PDOSC. This capability is independent of the chip's power-down state. Auto power-

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down mode and power-down via the POWER DOWN bit have no effect over the power state of the oscillator.

In the default state the PDOSC bit is low and the oscillator is powered up. When this bit is programmed to a 1, the oscillator is shut off. Hardware reset clears this bit to 0. Neither of the software resets has any effect on this bit. Note that PDOSC should be set high only when the part is in the power-down state; otherwise, the part will not function correctly and must be hardware reset once the oscillator has turned back on and stabilized.

Bits 2-4, PRECOMP 0-2, adjust the WRDATA output to the disk to compensate for magnetic media phenomena known as "bit shifting." The data patterns that are susceptible to bit shifting are well understood and the 82078 compensates the data pattern as it is written to the disk. The amount of precompensation is dependent upon the drive and media, but in most cases the default value is acceptable.

The 82078 starts precompensating the data pattern on Track 0. The CONFIGURE command can change the track on which precompensating starts. The following "Precompensation Delays" table lists the precompensation values that can be selected, and the "Default Precompensation Delays" table lists the default precompensation values. The default value is selected if the three bits are zeros.

Bits 0 and 1, DRATESEL 0-1, select one of the four data rates as listed in the "Data Rates" table below. The default value is 250 Kbps upon a chip reset. Other resets do not affect the DRATE or PRECOMP bits.

Data Rates

DRATESEL1	DRATESEL0	DATARATE
1	1	1 Mbps
0	0	500 Kbps
0	1	300 Kbps
1	0	250 Kbps

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Precompensation Delays

PRECOMP BITS 432	Precompensation Delay
111	0.00 ns -- DISABLED
001	41.67 ns
010	83.34 ns
011	125.00 ns
100	166.67 ns
101	208.33 ns
110	250.00 ns
000	DEFAULT

Default Precompensation Delays

Data Rate	Precompensation Delays
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
200 Kbps	125 ns

Main Status Register (MSR)

3F4h Default

The Main Status Register is a read-only register used to control command input and result output for all commands.

7	6	5	4	3	2	1	0
RQM	DIO	NON DMA	CMD BUSY	DRV 3 BUSY	DRV 2 BUSY	DRV 1 BUSY	DRV 0 BUSY

Main Status Register

RQM -- Indicates the host can transfer data if set to logical 1. No access is permitted if set to logical 0.

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DIO -- Indicates the direction of a data transfer once RQM is set. A 1 indicates a read is required and 0 indicates a write is required.

NON-DMA -- This mode is selected in the SPECIFY command and will be set to 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.

COMMAND BUSY -- This bit is set to 1 when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the result phase. If there is no result phase (SEEK, RECALIBRATE commands), this bit is returned to 0 after the last command byte.

DRV x BUSY -- These bits are set to 1 when a drive is in the seek portion of a command, including implied and overlapped seeks, and recalibrates.

Data (FIFO)

3F5h Default

All command parameter information and disk data transfers go through the FIFO. The FIFO is 16 bytes in size and has programmable threshold values. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to PC/AT compatible mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the CONFIGURE command (enable full FIFO operation with threshold control). The advantage of the FIFO is it allows the system a larger DMA latency without causing a disk error. The two "FIFO Service Delay" tables, below, give several examples of the delays with a FIFO. The data is based upon the following formula:

$$\text{Threshold\#} \times \left| \frac{1}{\text{DATARATE}} \times 8 \right| - 1.5\ \mu s = \text{DELAY}$$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the 82078 enters the command execution phase, it clears the FIFO of any data to ensure invalid data is not transferred.

An overrun or underrun terminates the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

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FIFO Service Delay

1 Mbps Data Rate

FIFO Threshold Examples	Maximum Delay to Servicing at 1 Mbps Data Rate
1 byte	1 x 8 µs - 1.5 µs = 6.5 µs
2 bytes	2 x 8 µs - 1.5 µs = 14.5 µs
8 bytes	8 x 8 µs - 1.5 µs = 62.5 µs
15 bytes	15 x 8 µs - 1.5 µs = 118.5 µs

500 Kbps Data Rate

FIFO Threshold Examples	Maximum Delay to Servicing at 500 Kbps Data Rate
1 byte	1 x 16 µs - 1.5 µs = 14.5 µs
2 bytes	2 x 16 µs - 1.5 µs = 30.5 µs
8 bytes	8 x 16 µs - 1.5 µs = 126.5 µs
15 bytes	15 x 16 µs - 1.5 µs = 238.5 µs

Digital Input Register (DIR)

3F7h Default

This register senses the state of the DSKCHG input and is read-only.

7	6	5	4	3	2	1	0
DSK CHG	ND†	ND†	ND†	ND†	ND†	ND†	ND†

† ND: Not driven by ZT 8954

Digital Input Register

Bit 7 , DSKCHG, monitors the pin of the same name and reflects the opposite value seen on the disk cable. **Bits 0-6** are not driven by the ZT 8954.

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Configuration Control Register (CCR)

3F7h Default

This register sets the data rate and is write only. In the PC/AT it is named the DSR.

7	6	5	4	3	2	1	0
—	—	—	IDLE-MASK	—	—	DRATE SEL1	DRATE SEL0

Configuration Control Register

Refer to the "Data Rates" table in the "Datarate Select Register" section of this chapter for values.

Bit 4, IDLEMASK, is used to mask the IDLE pin on the 82078, which is not used on the ZT 8954. Its use can be ignored and should be left enabled (logic 0).

Unused bits should be set to 0.

RESET

As discussed in the following topics, the 82078 has three sources of reset: the RESET pin; a reset generated via a bit in the DOR; and a reset generated via a bit in the DSR. All resets take the 82078 out of the power down state.

On entering the reset state, all operations are terminated and the 82078 enters an idle state. Activating reset while a disk write activity is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, including the CONFIGURE command information, and the 82078 waits for a new command. Drive polling will start unless disabled by a new CONFIGURE command.

RESET Pin

The RESET pin is a global reset and clears all registers except those programmed by the SPECIFY command. The DOR Reset bit is enabled and must be cleared by the host to exit the reset state.

DOR Reset vs. DSR Reset

These two resets are functionally the same. The DSR Reset is included to maintain 82072 compatibility. Both reset the 82078 core, which affects drive status information

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and the FIFO circuits. The DSR Reset clears itself automatically, while the DOR Reset requires the host to manually clear it. DOR Reset has precedence over the DSR Reset. The DOR Reset is set automatically upon a pin RESET. You must manually clear this reset bit in the DOR to exit the reset state.

DMA TRANSFERS

DMA transfers are enabled with the SPECIFY command and are initiated by the 82078 by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting DACK*.

COMMAND SET/DESCRIPTIONS

Commands can be written whenever the 82078 is in the command phase. Each command has a unique set of needed parameters and status results. The 82078 checks to see if the first byte is a valid command and if valid, proceeds with the command. Refer to the 82078 data sheet for details on the COMMAND SET.

ADDITIONAL INFORMATION

Refer to the Intel *Peripherals Data Book* for further details on the 82078-1 Floppy Disk Controller. When referring to the 82078-1 data sheet, it is important to note that the ZT 8954 is configured for PS/2 mode through the connection of IDENT1 and IDENT0. IDENT0 is grounded on the ZT 8954. IDENT1 is tied to Vcc. Also, note that the 82078-1 can be configured for either a 24 MHz crystal/oscillator or a 48 MHz oscillator. The ZT 8954 uses a 24 MHz crystal for internal timing. The 48 MHz oscillator option is not provided.

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A. JUMPER CONFIGURATIONS

The ZT 8954 includes several jumper options that tailor the operation of the board to the requirements of specific applications. Options are selected by installing and removing shorting receptacles (jumpers).

This appendix provides detailed descriptions of all jumper options, as well as an illustration of the board showing the locations of all jumpers.

JUMPER OPTIONS

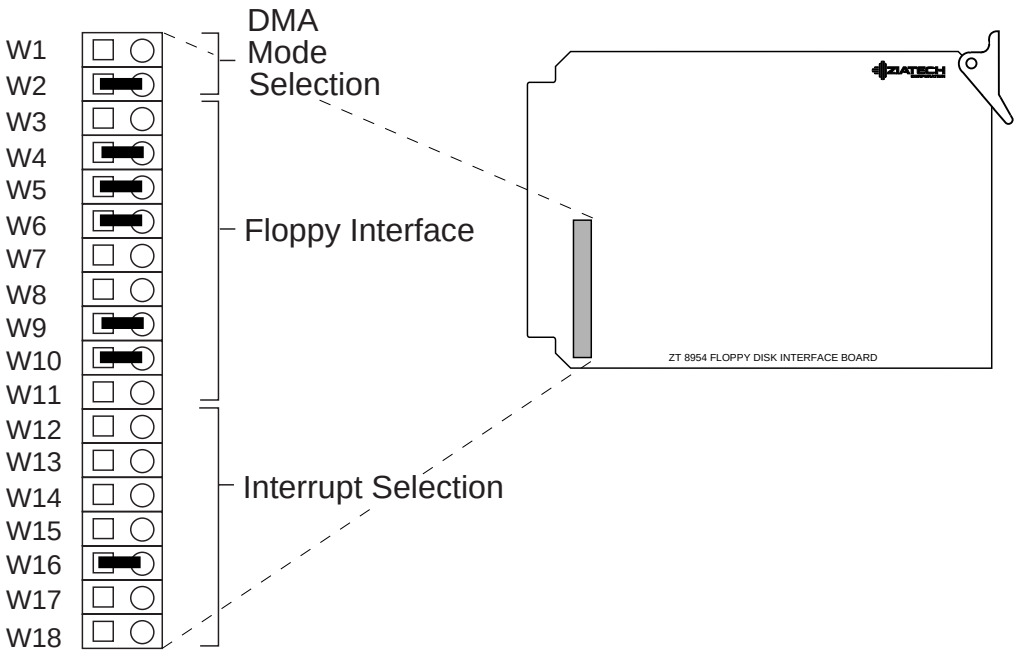
ZT 8954 jumper locations are illustrated in the "Customer Jumper Locations" figure; use this figure to document your jumper configuration if it differs from the factory default settings, illustrated in the "Factory Default Jumper Configuration" figure.

The "Jumper Cross Reference" table below divides the jumper options into functional groups.

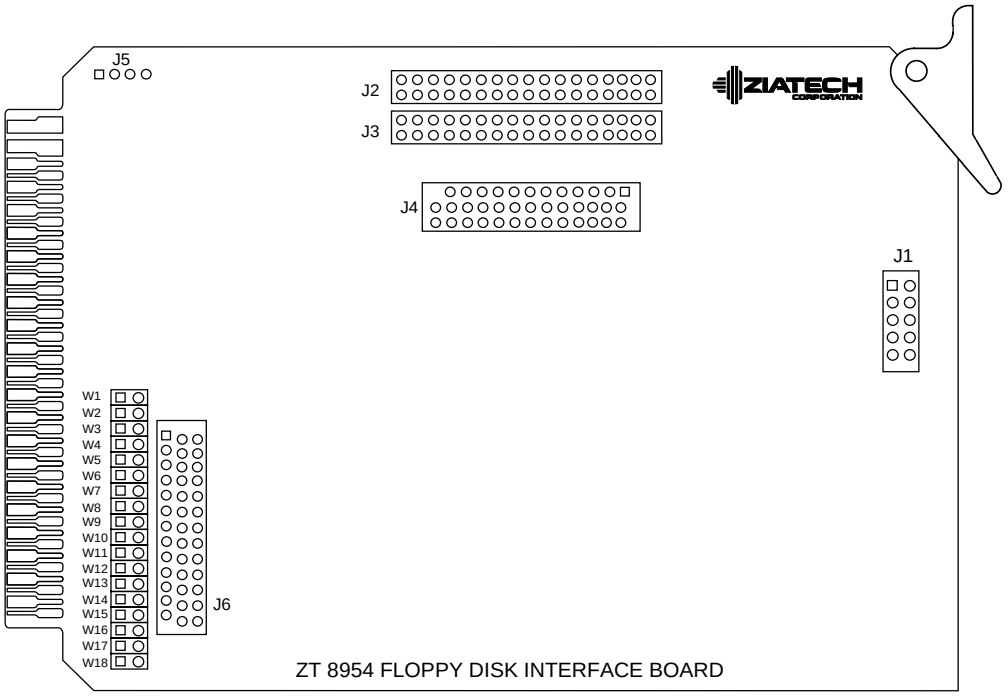
Jumper Cross Reference

Function	Jumpers
DMA Mode Selection	W1, W2
Floppy Interface	W3-W11
Interrupt Selection	W12-W18

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Factory Default Jumper Configuration



Customer Jumper Locations

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JUMPER DESCRIPTIONS

The following topics list the jumpers in numerical order and provide a detailed description of each jumper. A dagger (†) indicates the default jumper configuration.

W1-2 (DMA Mode Selection)

The ZT 8954 can be used in four DMA modes. The primary mode (Mode 2 DMA) uses the BUSRQ*/BUSAK* signals on the backplane for DMA request/acknowledge and uses the backplane control signals for the data transfer. The other modes allow configuration for slot-specific DMA (Mode 1), frontplane DMA (Mode 3), or a combination of frontplane and backplane signals for use in STD-80 backplanes (Mode 0).

The control signals are DMAIOR*, DMAIOW*, and T-C for the backplane and DMAW*, DMAR*, and TC* for the frontplane. Note that frontplane control is a factory option because the frontplane connector is not nominally loaded. Refer to the J1 (DMA PORT) topic in Appendix B, "Specifications."

W2	W1	Mode	Request/Ack.	Control Signals
Out	Out	0	BUSRQ*/BUSAK*	Frontplane
Out	In	1	DRQx*/DAKx*	Backplane
†In	†Out	2	BUSRQ*/BUSAK*	Backplane
In	In	3	Frontplane	Frontplane

† Factory default configuration

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W3-11 (Floppy Interface)

These jumpers select various options for the floppy interface. In general, these jumpers should not be changed from the factory default. These jumpers affect how the floppy disk controller interfaces to the floppy disk drive. ***Do not install jumpers W6 and W7 together, nor W8 and W9 together, nor W10 and W11 together.***

Jumper Installed	Description
W3	DRV2 The state of this jumper is reflected in Status Register A (3F0h)
†W4	DRVID0 This bit is reflected in the Tape Drive Register (3F3h)
†W5	DRVID1 This bit is reflected in the Tape Drive Register (3F3h)
†W6	Invert DRVDEN0 to floppy drive when in
W7	Drive DRVDEN0 to floppy drive directly (non-inverted)
W8	Invert DRVDEN1 to floppy drive when in
†W9	Drive DRVDEN1 to floppy drive directly (non-inverted)
†W10	Drive Write protect circuitry with WE* from FDC
W11	Factory Test option. Do not install with W10 installed

W12-18 (Interrupt Selection)

These jumpers allow the floppy disk drive interrupt to be routed to any of the backplane interrupts on the STD/STD 32 bus (see the "Interrupt Selections" illustration in Chapter 3). DOS-based systems use IR6 for floppy disk drive interfacing. Be sure to configure the CPU board for this option. Ziatech uses INTRQ2*, by default, for floppy disk subsystem interrupts.

Jumper Installed	Backplane Connection
W12	IRQx* (Active HIGH) E47
W13	IRQx* (Active LOW) E47
W14	INTRQ* P44
W15	INTRQ1* P37
†W16	INTRQ2* P50
W17	INTRQ3* E67
W18	INTRQ4* P5 (VBAT)

† Factory default configuration

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B. SPECIFICATIONS

This appendix contains the electrical, environmental, and mechanical specifications for the ZT 8954 Low Profile Floppy Disk Controller.

ELECTRICAL AND ENVIRONMENTAL

This section provides tables showing the following:

- Absolute maximum ratings
- DC operating characteristics
- STD bus loading characteristics

Note: Integrated Floppy references are for the Sony MPF320-01 slimline drive.

Absolute Maximum Ratings

Supply Voltage, Vcc: 0 to 7 V

Supply Voltage, AUX +V: 0 to 13 V

Storage Temperature

ZT 8954-D0: -40º to +85º C

ZT 8954-D1 (Integrated Floppy): -20º to +60º C

Operating Temperature

ZT 8954-D0: 0º to +65º C

ZT 8954-D1: +5º to +50º C

DC Operating Characteristics

Supply Voltage, Vcc: 4.75 to 5.25 V

Supply Voltage, AUX +V: 11.4 to 12.6 V

Supply Current, +12 V: None[‡]

[‡] +12 V may be required if remote drive is used and requires +12 V. +12 V is supplied through J5 to the remote drive.

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Supply Current, Vcc

ZT 8954-D0: 105 mA typ, 250 mA maximum

ZT 8954-D1: 110 mA typ, 800 mA maximum†

Non-condensing relative humidity

ZT 8954: <95 percent @ 40º C

ZT 8954 (Integrated Floppy): 8 to 80 percent @ 29º C

STD-80 Compatibility

The ZT 8954 is designed for use in an STD 32 backplane environment. While designed to be backward compatible with STD-80 systems, the ZT 8954 is not guaranteed to work in all system topologies.

STD Bus Loading Characteristics

The unit load is a convenient method for specifying the input and output drive capability of STD bus cards. In the STD bus systems, one unit load is equal to one LSTTL load as follows:

Maximum high level input current: 20 µAmps

Maximum low level input current: -400 µAmps

The STD bus unit load reflects input current requirements at worst case conditions over the recommended supply voltage and ambient temperature ranges. An output rate at 60 unit loads can drive 60 STD bus cards having input rated at one unit load.

The following "STD 32 Bus Loading, P Connector" table shows load values for STD-80 signals (P signals). The following "STD 32 Bus Loading, E Connector" table shows load values for signals used in STD 32 systems (E signals).

† Maximum values are for motor start and step operations.

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STD 32 Bus Loading, P Connector

PIN (CIRCUIT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC							PIN (COMPONENT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC
+5 VOLTS [A]			2	1			+5 VOLTS [A]
GROUND			4	3			GROUND
DCPDN* [NC]			6	5			VBATT [NC]
D7 (A23) [C]	1	59	8	7	59	1	D3 (A19) [C]
D6 (A22) [C]	1	59	10	9	59	1	D2 (A18) [C]
D5 (A21) [C]	1	59	12	11	59	1	D1 (A17) [C]
D4 (A20) [C]	1	59	14	13	59	1	D0 (A16) [C]
A15	1		16	15			A7
A14	1		18	17			A6
A13	1		20	19			A5
A12	1		22	21			A4
A11	1		24	23		1	A3
A10	1		26	25		2	A2
A9	1		28	27		2	A1
A8	1		30	29		2	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
BHE			36	35			IOEXP
ALE*			38	37	60		INTRQ1*
STATUS 0*			40	39			STATUS 1*
BUSRQ*		60	42	41		1	BUSAK*
INTRQ*		60	44	43			INTAK* [NC]
NMIRQ*			46	45			WAITRQ*
PBRESET* [NC]			48	47		1	SYSRESET*
INTRQ2* (CNTRL*)	1	60	50	49		1	CLOCK*
PCI [B]			52	51			PCO [B]
AUX GND			54	53			AUX GND
AUX-V			56	55			AUX+V

Notes to the STD Bus Loading Diagram

[A] is the logic supply drain = 2.0 Amps max.

[B] PCI and PCO are shorted together.

[C] High order address bits multiplexed over data bus D0-D7.

[NC] No Connection.

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STD 32 Bus Loading, E Connector

PIN (CIRCUIT SIDE) OUTPUT DRIVE INPUT LOAD MNEMONIC							PIN (COMPONENT SIDE) OUTPUT DRIVE INPUT LOAD MNEMONIC
RSVD XA23 XA22 XA21			E2 E4 E6 E8	E1 E3 E5 E7			GND XA19 XA18 XA17
XA20 RSVD +5V DREQX*		60	E10 E12 E14 E16	E9 E11 E13 E15		1	XA16 NOWS* +5V DAKx*
GND D31 D30 D29			E18 E20 E22 E24	E17 E19 E21 E23			GND D27 D26 D25
D28 GND D15 D14			E26 E28 E30 E32	E25 E27 E29 E31			D24 D23 D22 D21
D13 D12 D11 D10			E34 E36 E38 E40	E33 E35 E37 E39			D20 GND D19 D18
D9 D8 MASTER16* AENX*			E42 E44 E46 E48	E41 E43 E45 E47			D17 D16 GND IRQx
BE3* BE2* GND W-R			E50 E52 E54 E56	E49 E51 E53 E55			BE1* BE0* MEM16* M-IO
DMAIOR* EX8* START* EX32*	1		E58 E60 E62 E64	E57 E59 E61 E63		1	DMAIOW* IO16* CMD* EX16*
T-C +5V MREQx* MSBURST*	1		E66 E68 E70 E72	E65 E67 E69 E71			EXRDY INTRQ3* MAKx* SLBURST*
XA31* XA30* XA29* XA28*			E74 E76 E78 E80	E73 E75 E77 E79			XA27* XA26* XA25* XA24*

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MECHANICAL

This section includes the following mechanical specifications:

- Card dimensions and weight
- Connectors (including connector locations, descriptions, and pinouts)
- Cables showing dimensions for building cables to interface with the ZT 8954

Card Dimensions And Weight

The ZT 8954 meets the *STD 32 Bus Specification* for all mechanical parameters. In a card cage with 0.625" spacing, the ZT 8954 requires one card slot as a stand-alone card. As an integrated Floppy Disk Controller, the ZT 8954 also requires just one slot.

The figure "Board Dimensions" shows the mechanical dimensions of the ZT 8954.

The ZT 8954-D3 requires three STD card slots.

Board Length: 16.51 cm ± 0.063 cm (6.500 in ± 0.005 in)

Board Width: 11.43 cm ± 0.038 cm (4.500 in ± 0.005 in)

Board Thickness: 0.158 cm ± 0.013 cm (0.062 in ± 0.007 in)

Board Weight:

ZT 8954-D0: 200 g (7 oz)

ZT 8954-D1 (Integrated Floppy): 624 g (22 oz)

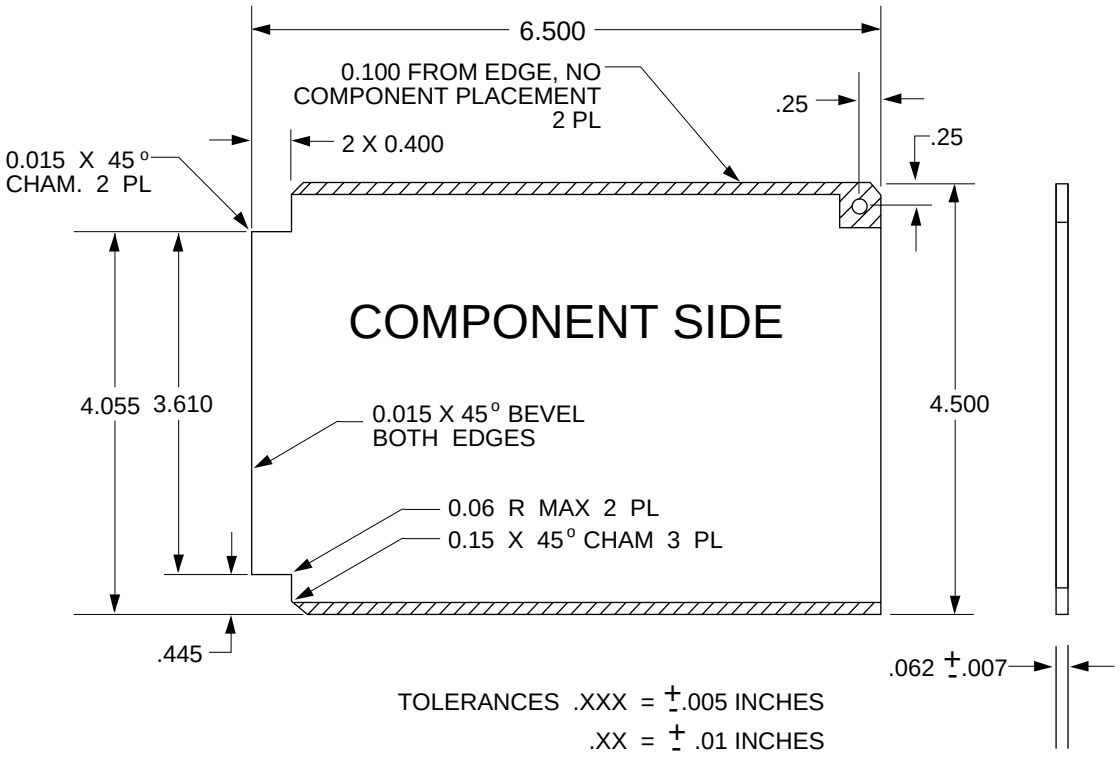
Board Height From Top Surface:

ZT 8954-D0: 0.953 cm (0.375 in) maximum

ZT 8954-D1: 1.27 cm (0.5 in) maximum

Board Height From Bottom Surface: 0.102 cm (0.040 in) maximum

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Board Dimensions

Connectors

As shown in the "Connector Locations" illustration, the ZT 8954 includes six connectors to interface to the STD bus and application-specific devices. The following topics provide descriptions of the individual connectors. Connector assignments are listed below.

P and E: STD-80 bus and STD 32 bus, respectively

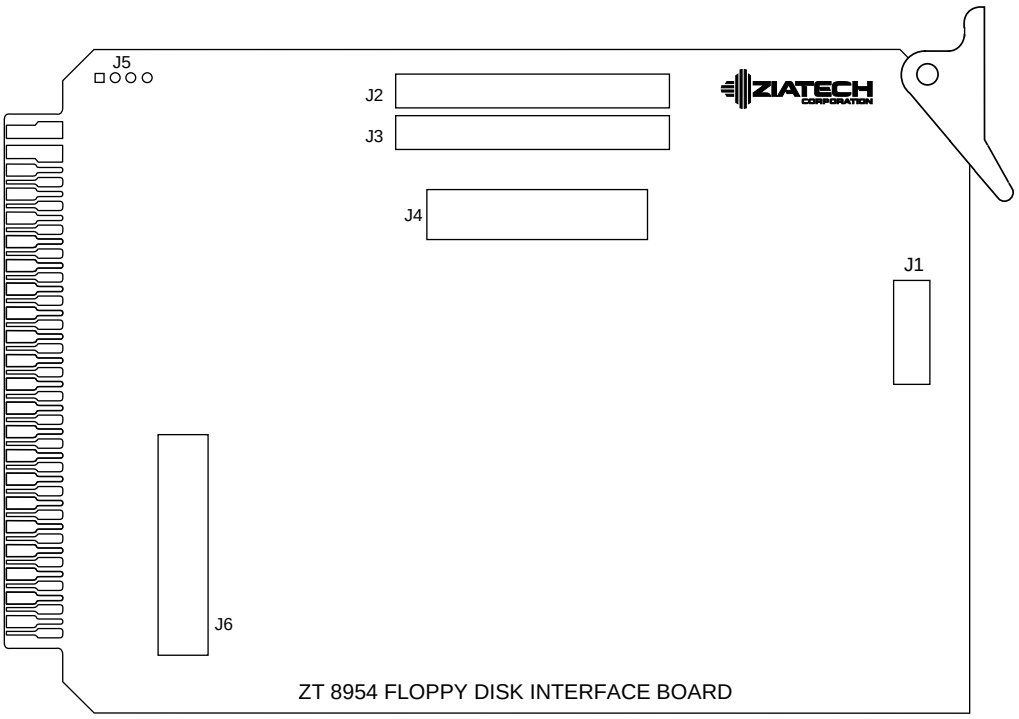
J1**:** DMA

J2, J3**:** 0.1" 34-pin floppy interface drives

J4, J6**:** 1 mm FPC cable connectors for slimline floppy disk drives

J5**:** Power cable connector for remote floppy disk drives

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Connector Locations

STD 32 P/E Connector

P: The P connector is the interface between the ZT 8954 and the STD-80 bus. This connector is a 56-pin (dual 28-pin) card-edge connector with fingers on 0.125 inch contact spacing. The mating connector is a Viking 3VH28/1CNK5 or equivalent for the solder tail, or a Viking 3VH28/1CND5 or equivalent for a three-level wire wrap.

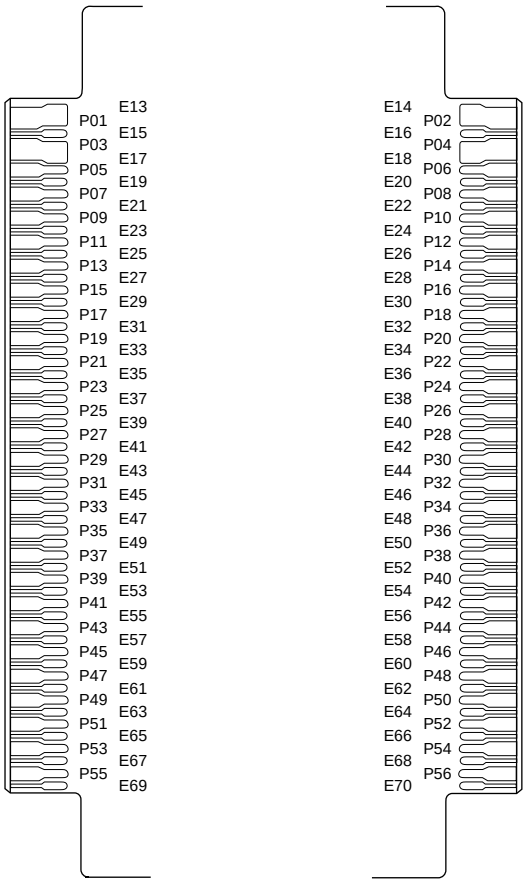
E: The E connector extends the P connector to interface the ZT 8954 to the STD 32 bus. This connector combines with the P connector to make a 114-pin (dual 57-pin) card-edge connector with fingers on 0.0625 inch contact spacing. The mating connector is a Viking S3VT68/5DP12 or equivalent for the solder tail, or a Viking S3VT68/5DE12 or equivalent for the card extender.

Pinouts: The following "STD 32 P/E Connector Pinout" illustration shows pin assignments for the P and E connectors.

The "STD 32 Bus Loading, P Connector" table shows P connector signal assignments.

The "STD 32 Bus Loading, E Connector" table shows E connector signal assignments.

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(Component Side) (Solder Side)

STD 32 P/E Connector Pinout

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J1 (DMA Port)

J1 is a latching 10-pin (dual 5-pin) male transition connector with 0.1 inch lead spacing. J1 provides Direct Memory Access (DMA) support for external peripherals via channel 0 or 3 on the local 8237A DMA controller. Jumpers W1 and W2 control configuration of this connector. Refer to the W1-2 description in Appendix A, "Jumper Configurations," for further details. Pin assignments are given in the following "J1 DMA Port Pinout" table. The floppy disk controller can use this connector to request service from the DMA controller on the ZT 8954. The mating connector is a T&B Ansley #622-1030. This connector is not normally loaded on the ZT 8954, as it resides under the integrated floppy drive.

J1 DMA Port Pinout

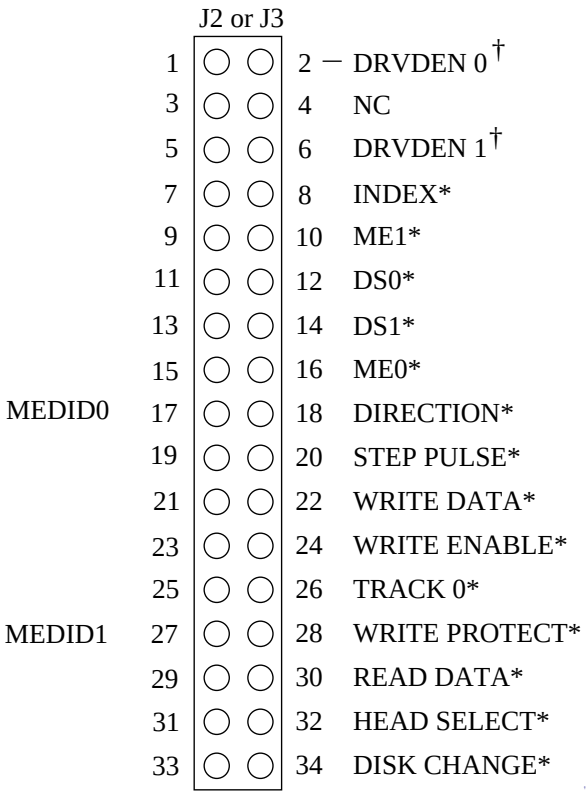
Pin	Signal	Description
2	DRQ*	DMA Request
4	DAK*	DMA Acknowledge
6	DMAW*	DMA Write
8	DMAR*	DMA Read
10	T/C*	Terminal Count
9	GND	Ground
1,3,5,7	NC	No Connect

Note: Signals ending with an asterisk (*) are active low; those without are active high.

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J2, J3 (Floppy Interface)

Although not located directly on the front edge of the ZT 8954, J2 and J3 are described in this section. These connectors accommodate 0.1" 34-pin floppy interface drives. The pinouts are given in the "J2 and J3 Pinout (Top View)" illustration below. J3 is a reverse image of J2 to allow interfacing to drives with minimal cable twisting.



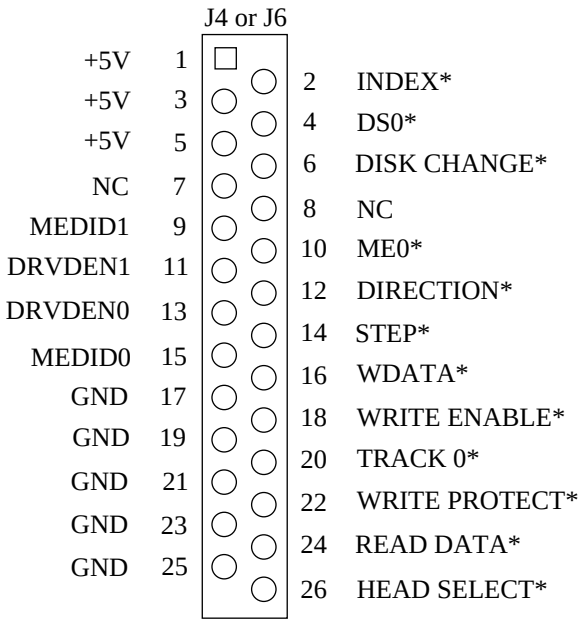
J2 and J3 Pinout (Top View)

† The polarities of DRVDEN1 and DRVDEN0 are selectable via W6-9; consult Appendix A for details.

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J4, J6 (Slimline Floppy Disk Drive)

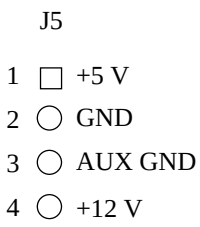
J4 and J6 are 1 mm FPC cable connectors for newer slimline floppy disk drives. The pinouts are given below in the "J4 and J6 Pinout (Top View)" illustration. J4 is not loaded by default as it is underneath the integrated floppy drive. Interfacing cables are available from Parlex , which can be reached by phone at (603) 893-0040. Specify 1 mm FPC cable. Cables can be up to 0.5 meters in length.



J4 and J6 Pinout (Top View)

J5 (Power Cable)

J5 is for a power cable connection location for remote floppy disk drives. The following figure "J5 Pinout (Top View)" illustrates the pinout for these locations.



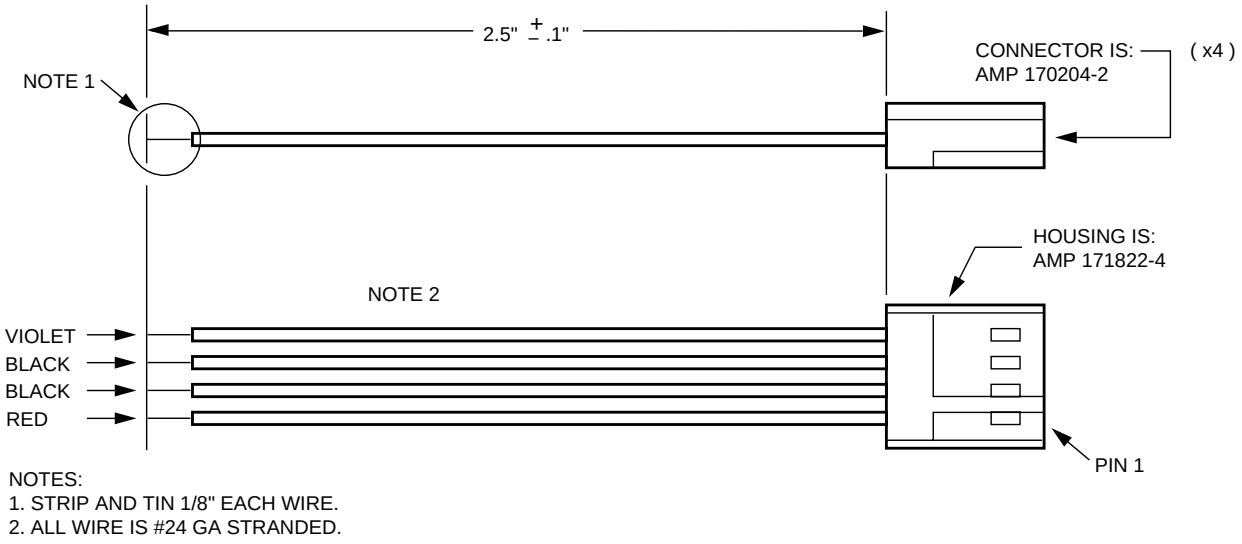
J5 Pinout (Top View)

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Cables

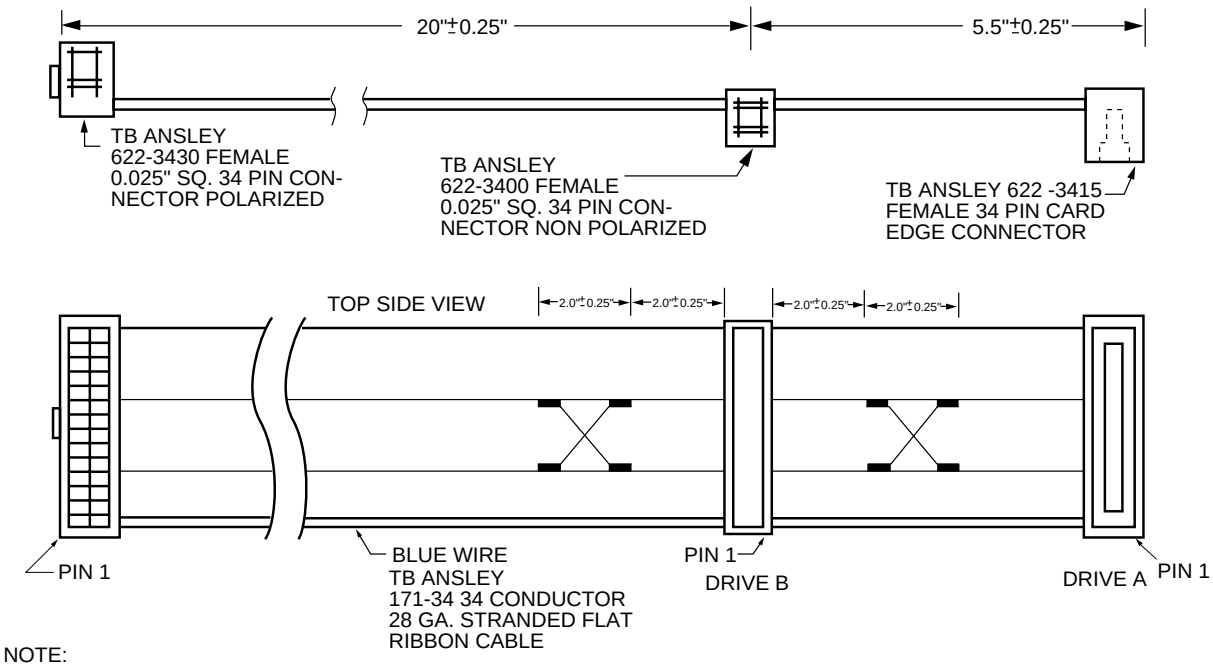
The following cables are available from Ziatech Corporation. Cable drawings are included here for those who wish to make their own cables.

- ZT 90025 2.5" power cable
- ZT 90077 Optional; floppy 20-inch cable for connecting non-integrated 3½" and 5¼" floppy drives to the ZT 8954 controller
- ZT 90172 20" power cable



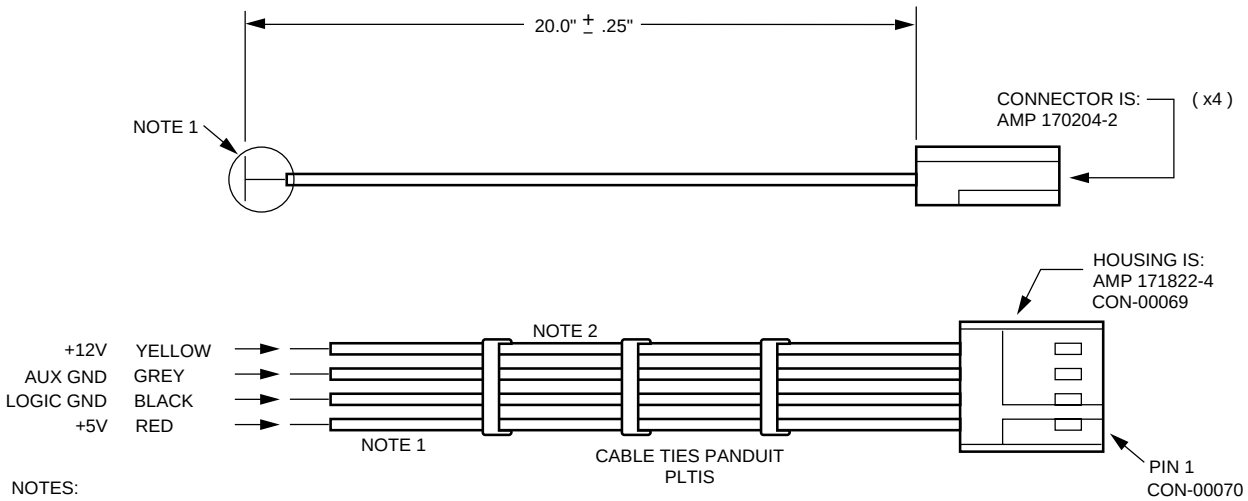
ZT 90025 Power Cable

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NOTE:
1. PINS 10 THRU 16 OF CABLE ARE TWISTED BETWEEN EACH CONNECTOR.
2. THICK LINES INDICATE WHERE TO SEPARATE CABLE FOR TWIST.

ZT 90077 Floppy 20-Inch Cable



NOTES:
1. ALL WIRE IS #20 AWG, 19/32 STRANDING, UL STYLE 1569, 105° C, AND 300V RATED.
2. TIE WRAPS ARE TO BE SPACED 1 1/2" FROM THE CONNECTORS AND HOUSING AND 4" FROM EACH OTHER. A TOTAL OF 6 TIES ARE USED.

ZT 90172 Power Cable

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C. CUSTOMER SUPPORT

This appendix offers technical assistance and warranty information for this product, and information on returning a Ziatech product for service.

TECHNICAL/SALES ASSISTANCE

If you have a technical question, please call Ziatech's Customer Support Service at the number below, or e-mail our technical support team at tech_support@ziatech.com. Ziatech also maintains an FTP site located at ftp://ziatech.com/Tech_support.

If you have a sales question, please contact your local Ziatech Sales Representative or the Regional Sales Office for your area. Address, telephone and FAX numbers, and additional information are available at Ziatech's website, located at http://www.ziatech.com.

Corporate Headquarters

1050 Southwood Drive

San Luis Obispo, CA 93401 USA

Tel (805) 541-0488

FAX (805) 541-5088

RELIABILITY

Ziatech takes extra care in the design of the ZT 8954 in order to ensure reliability. The product was designed in top-down fashion, using the latest in hardware and software design techniques, so that unwanted side effects and unclean interactions between parts of the system are eliminated. Each ZT 8954 has an identification number. Ziatech maintains a lifetime data base on each board and the components used. Any negative trends in reliability are spotted and Ziatech's suppliers are informed and/or changed.

RETURNING FOR SERVICE

Before returning any of Ziatech's products, you must phone Ziatech at (805) 541-0488 and obtain a Return Material Authorization (RMA) number. Please supply the following information to Ziatech in order to receive an RMA number:

- Your company name and address for invoice
- Your shipping address and phone number
- The product I.D. number
- The name of a technically qualified individual at your company familiar with the mode of failure

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Once you have an RMA number, follow these steps to return your product to Ziatech:

1. Contact Ziatech for pricing if the warranty expired.

2. Supply a purchase order number for invoicing the repair if the warranty expired.

3. Pack the board in **anti-static** material and ship in a sturdy cardboard box with enough packing material to adequately cushion it.

Note: Any product returned to Ziatech improperly packed will immediately void the warranty for that particular product!

4. Mark the RMA number clearly on the outside of the box.

ZIATECH WARRANTY

Warranty information for Ziatech products is available at Ziatech's website, located at http://www.ziatech.com.

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1050 Southwood Drive
San Luis Obispo, CA 93401 USA
Tel: (805) 541-0488
FAX: (805) 541-5088
E-Mail: tech_support@ziatech.com
Internet: http://www.ziatech.com

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